SPECTRUM DIGITAL INCORPORATED

TMS320DM355 Evaluation Module

Technical Reference

2008 ***DSP Development Systems***

TMS320DM355 Evaluation Module Technical Reference

509905-0001 Rev. E
April 2008

SPECTRUM DIGITAL, INC.
12502 Exchange Drive, Suite 440 Stafford, TX. 77477
Tel: 281.494.4505 Fax: 281.494.5310
sales@spectrumdigital.com www.spectrumdigital.com

IMPORTANT NOTICE

Spectrum Digital, Inc. reserves the right to make changes to its products or to discontinue any product or service without notice. Customers are advised to obtain the latest version of relevant information to verify that the data being relied on is current before placing orders.

Spectrum Digital, Inc. warrants performance of its products and related software to current specifications in accordance with Spectrum Digital's standard warranty. Testing and other quality control techniques are utilized to the extent deemed necessary to support this warranty.

Please be aware that the products described herein are not intended for use in life-support appliances, devices, or systems. Spectrum Digital does not warrant nor is Spectrum Digital liable for the product described herein to be used in other than a development environment.

Spectrum Digital, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does Spectrum Digital warrant or represent any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Spectrum Digital, Inc. covering or relating to any combination, machine, or process in which such Digital Signal Processing development products or services might be or are used.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures necessary to correct this interference.

Contents

1 Introduction to the DM355 Evaluation Module 1-1
Provides you with a description of the DM355 Evaluation Module, key features, and block diagram.
1.1 Key Features 1-2
1.2 Functional Overview of the DM355 EVM 1-4
1.3 Basic Operation 1-4
1.4 Memory Map 1-5
1.5 Configuration Switch Settings 1-6
1.6 Power Supply 1-6
2 Board Components 2-1
Describes the operation of the major board components on the DM355 Evaluation Module.
2.1 EMIF Interfaces 2-2
2.1.1 Flash, NAND Flash, Ethernet Interface 2-2
2.1.2 DDR2 Memory Interface 2-2
2.1.3 Memory Card Interface 2-2
2.1.4 UART Interface 2-2
2.1.5 USB Interface 2-3
2.2 Input Video Port Interfaces 2-3
2.2.1 On Chip Video Output DAC 2-3
2.2.2 AIC33 Interface 2-4
2.3 Ethernet Interface 2-5
2.4 I^2C Interface 2-5
2.4.1 MSP430 2-6
2.5 Daughter Card Interface 2-6
2.6 DM355 CPU Video Clocks 2-6
2.7 Battery 2-7

3 Physical Specifications 3-1
Describes the physical layout of the DM355 Evaluation Module and its connectors.
3.1 Board Layout 3-3
3.2 Connectors 3-5
3.2.1 J1, NTSC/PAL Select 3-6
3.2.2 J2, Video In 3-7
3.2.3 J3, MSP430 JTAG Header 3-7
3.2.4 J4, Composite Video Out 3-8
3.2.5 J5, USB Connector 3-8
3.2.6 J6, 14 Pin External JTAG Connector 3-9
3.2.7 J8, ARM JTAG Emulation Header 3-10
3.2.8 J9, USB Capacitance Select 3-10
3.2.9 J10, USB ID Select 3-11
3.2.10 J11, S-Video In 3-11
3.2.11 J12, ATA/CE Interface 3-12
3.2.12 J16, +5 Volt Input 3-13
3.2.13 J27, MMC/SD Connector 3-13
3.2.14 J28, MMC/SD Connector 3-14
3.2.15 J30, Imager Interface Connector 1 3-15
3.2.16 J31, Imager Interface Connector 2 3-16
3.2.17 P1, Microphone In 3-16
3.2.18 P2, Headphone Out 3-17
3.2.19 P3, Line Out 3-17
3.2.20 P4, RS-232 UART 3-18
3.2.21 P5, Ethernet Interface 3-19
3.2.22 P6, Line In 3-20
3.2.23 DC3, I/O Daughter Card Expansion 3-21
3.2.24 DC5, TH8200 Daughter Card Interface 3-22
3.2.25 DC6, Expansion Connector 3-23
3.2.26 DC7, Expansion Connector 3-23
3.2.27 U10, Infrared Interface 3-24
3.3 LEDs 3-24
3.4 Switches 3-25
3.4.1 SW1, EMU0/1 Select Switch 3-25
3.4.2 SW5, Reset Switch 3-26
3.4.3 SW6, User Readable 4 Position DIP Switch 3-26
3.4.4 SW7, ARM Boot Mode Select 3-27
3.4.5 SW10 - SW14 3-27
3.5 Test Points 3-28
A Schematics A-1
Contains the schematics for the DM355 Evaluation Module
B Mechanical Information B-1
Contains the mechanical information about the DM355 Evaluation Module

About This Manual

This document describes the board level operations of the DM355 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM355 Processor.

The DM355 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM355 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM355 Evaluation Module will sometimes be referred to as the DM355 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the TMS320DM355 can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Production Release
B	Updated Figures
C	Edited text
D	Updated schematics
E	Updated schematics, Silkscreens, Figures

Table 2: Board History

PWB Revision	History
A	Production Release
B	Updated Silk-screen
C2	0.55 mm. Production Release
D2	0.65 mm. Production Release

Chapter 1

Introduction to the DM355 EVM

Chapter One provides a description of the DM355 EVM along with the key features and a block diagram of the circuit board.

Topic **Page**

1.1	**Key Features**	**1-2**
1.2	**Functional Overview of the DM355 EVM**	**1-4**
1.3	**Basic Operation**	**1-4**
1.4	**Memory Map**	**1-5**
1.5	**Configuration Switch Settings**	**1-6**
1.6	**Power Supply**	**1-6**

1.1 Key Features

The DM355 EVM is a standalone development platform that enables users to evaluate and develop applications for the TMS320DM355 processor. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

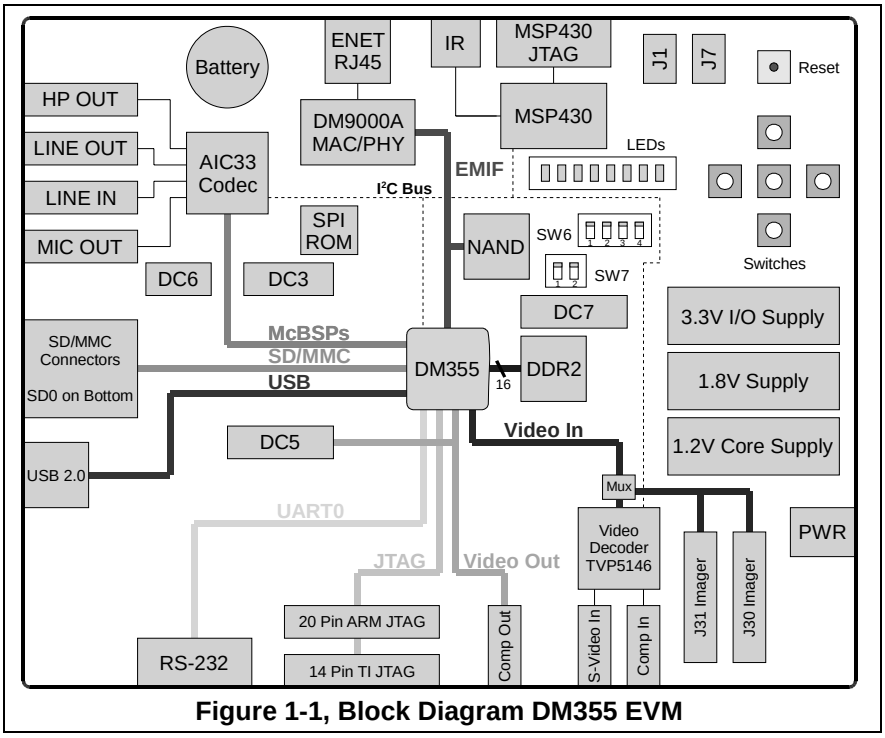


Figure 1-1, Block Diagram DM355 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM355 processor with an ARM processor operating up to 216 Mhz.
- 1 video input port, supports composite or S video
- 1 composite video DAC output
- 128 Mbytes of DDR2 DRAM
- UART, 2 SD/MMC card interfaces or 1 SD/MMC and 1 CE-ATA Disk Drive Interface
- 2 Gigabytes NAND Flash
- AIC33 stereo codec
- USB2 Interface

- 10/100 MBS Memory Mapped Ethernet Controller
- SPI EEPROM
- IR Remote Interface, real time clock, via MSP430
- Configurable boot load options
- 8 user LEDs/4 position user DIP switch/5 user push button switches
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- 14 Pin TI JTAG/20 Pin ARM JTAG Interfaces

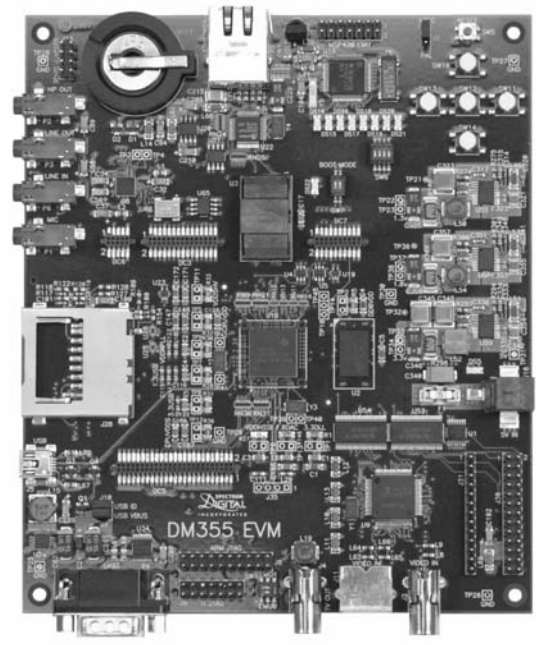


Figure 1-2, DM355 EVM

1.2 Functional Overview of the DM355 EVM

The DM355 on the EVM interfaces to on-board peripherals through the 8/16-bit wide EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 16 bit wide bus. The EMIF bus is also connected to the NAND Flash and ethernet controller.

On board video decoder and on chip encoder interface video streams to the DM355 processor. One decoder and 1 on chip DAC channel are standard on the EVM. On screen display functions are implemented in software on the DM355 processor.

An on-board AIC33 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 8 user LEDs, a 4 position user DIP switch, an IR interface, a Real time clock along with 5 user push button switches to provide the user with application interaction. These interfaces are implemented via software on a MSP430 and are accessed by reading and writing to the I^2C registers.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.3V CPU core voltage, +3.3V for peripherals and +1.8V for DDR2 memory. The board is held in reset by the on board MSP430 microcontroller until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an external emulator via the 14 pin external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

1.4 Memory Map

The DM355 processor has a byte addressable address space. There are some limitations to byte addressing which are determined by peripheral interconnection to the DM355 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic DM355 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 2 separate addressable regions called chip enable spaces (CE0 & CE1). The NAND Flash and ethernet controller are mapped into these chip enable spaces.

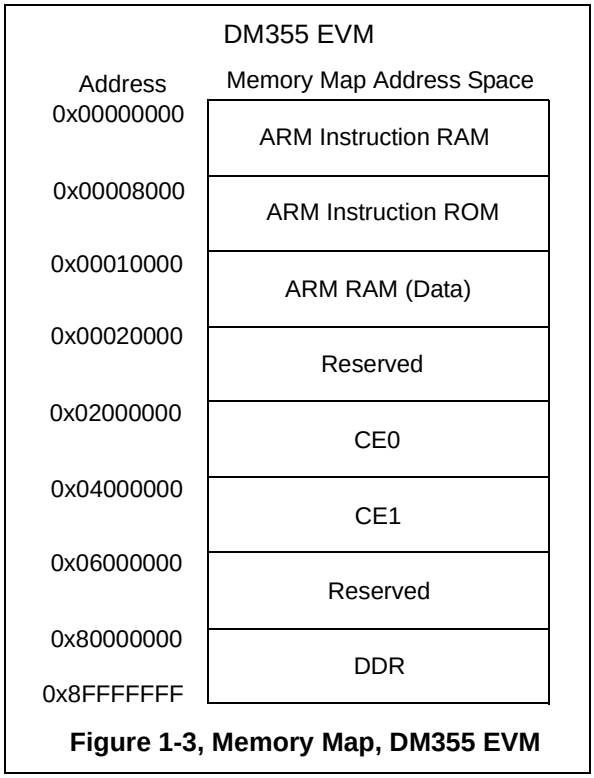


Figure 1-3, Memory Map, DM355 EVM

Shown below is a break out of the memory spaces.

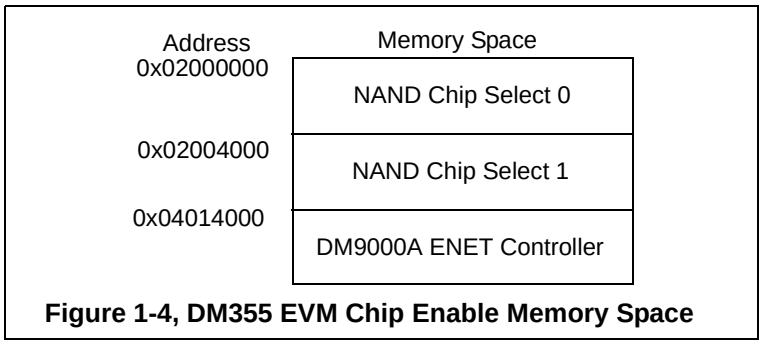


Figure 1-4, DM355 EVM Chip Enable Memory Space

1.5 Configuration Switch Settings

The EVM has a configuration switch that allow users to control the operational state of the processor when it is released from reset and determine the source for processor booting. Switch SW7 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to NAND Flash boot. The EMIF configuration switch must be set accordingly.

Table 1: SW7, Boot Mode Select

Pos 2	Pos 1	Boot Pin BTSEL1/BTSEL0	Function
ON	ON	0 0	NAND boot CE0 *
ON	OFF	0 1	Not Supported
OFF	ON	1 0	Boot from SD/MMC
OFF	OFF	1 1	Boot from UART

* Default Setting

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J14), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.3V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM355 DDR2 memory.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM355 EVM.

Topic **Page**

2.1	EMIF Interfaces	2-2
2.1.1	Flash, NAND Flash, Ethernet Interface	2-2
2.1.2	DDR2 Memory Interface	2-2
2.1.3	Memory Card Interface	2-2
2.1.4	UART Interface	2-3
2.1.5	USB Interface	2-3
2.2	Input Video Port Interfaces	2-3
2.2.1	On Chip Video Output DAC	2-3
2.2.2	AIC33 Interface	2-4
2.3	Ethernet Interface	2-5
2.4	I^2C Interface	2-5
2.4.1	MSP430	2-6
2.5	Daughter Card Interface	2-6
2.6	DM355 CPU/Video Clocks	2-6
2.7	Battery	2-7

2.1 EMIF Interfaces

A separate 16 bit EMIF with two chip enables divide up the address space and allow for asynchronous accesses on the EVM.

2.1.1 Flash, NAND Flash, Ethernet Interface

The DM355 has 2 gigabytes of NAND Flash memory, and an ethernet interface memory mapped into the CE0 and CE1 spaces. The NAND Flash memory is used primarily for boot loading and file system on the DM355 EVM. The CE0 and CE1 space are configured as 8 and 16 bits wide respectively on the DM355 EVM.

2.1.2 DDR2 Memory Interface

The DM355 device incorporates a dedicated 16 bit wide DDR2 memory bus. The EVM uses one gigabit 16 bit wide memories on this bus, for a total of 128 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. Memory refresh for DDR2 is handled automatically by the DM355 internal DDR controller.

2.1.3 Memory Card Interface

The EVM supports two (2) SD/MMC media card interfaces. The second SD connector is connected in parallel to the CE-ATA disk drive connector.

2.1.4 UART Interface

The internal UART0 on the DM355 device is driven to connector P4. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, P4.

2.1.5 USB Interface

The DM355 incorporates an on chip USB II controller. This interface is brought out to a mini A/B connector with its own power regulator. Two jumpers are provided to make a flexible host peripheral, and USB on the go interface.

2.2 Input Video Port Interfaces/Imager Input Ports

The DM355 EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device. J11 is used for the S-video inputs and J2 for the composite inputs on the EVM.

The input port can also be driven by LCD imagers connected to connectors J30 and J31. The imager or encoder is selectable via software control on I^2C bus by accessing MSP430 registers.

2.2.1 On Chip Video Output DAC

The DM355 incorporates 1 composite video output DAC to interface to various video output standards. The DAC is filtered and driven to RCA jack, J4.

2.2.2 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the AIC33's control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

McBSP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked via a 27 Mhz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM355 EVM.

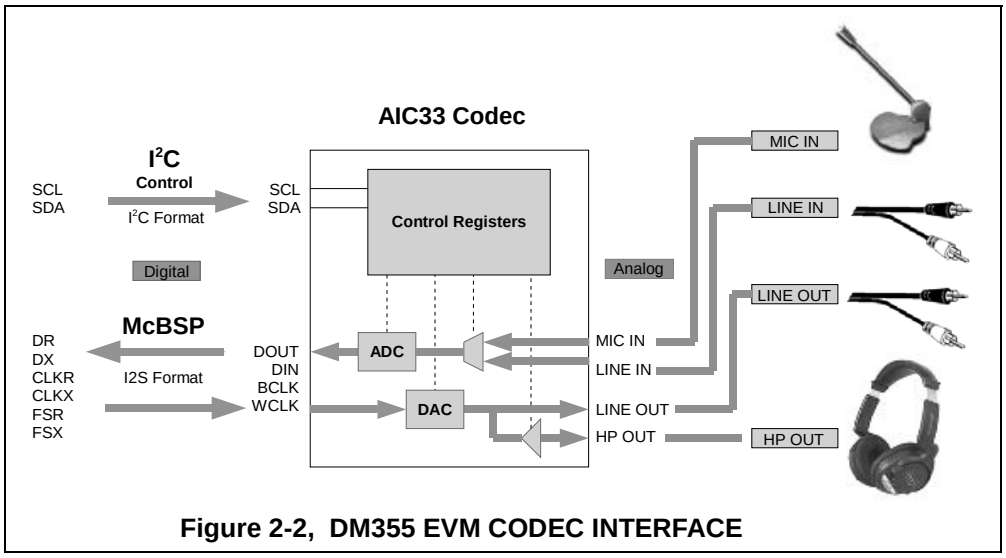


Figure 2-2, DM355 EVM CODEC INTERFACE

2.3 Ethernet Interface

The DM355 EVM incorporates an ethernet controller chip. This interface is connected to the DM355's EMIF. The EVM uses an Intel DAVICOM DM9000A. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P5. The ethernet address is stored in the ethernet controller's SPI ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

2.4 I^2C Interface

The I^2C bus on the DM355 is ideal for interfacing to the control registers of many devices. On the DM355 EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders, and communicate with the MSP430. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

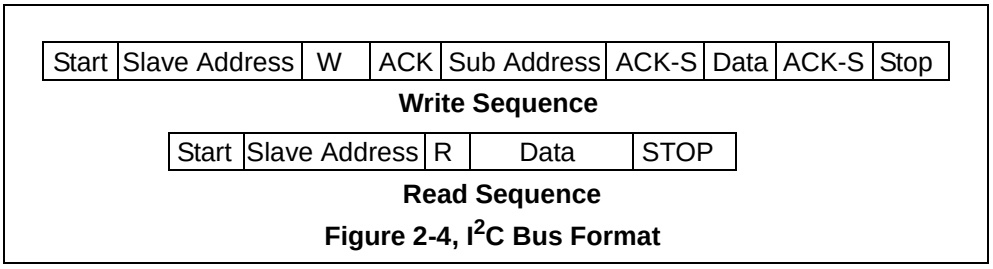


Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 1: I^2C Memory Map

Device	Address	R/W	Function
TVP5146	0x5D	R/W	Capture 1 Decoder
TLV320AIC33	0x1B	R/W	CODEC
MSP430	0x25	R/W	LEDs, IR, RTC, User I/O

2.4.1 MSP430

The DM355 EVM incorporates infrared remote, real time clock, and user and system bit I/O in a MSP430 microcontroller. The I^2C interface is used on the DM355 processor to communicate to the MSP430. The MSP430 acts as a slave device on the I^2C bus.

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are interfaces which include McBSP, and serial I/O expansion. The unused EMIF signals are brought out as user GPIO signals. The video output port is brought out to the daughter card interface along with I/O and imager interface.

2.6 DM355 CPU/Video Clocks

The DM355 EVM uses a 24 Megahertz crystal to generate the main input clock. The DM355 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM355 device.

The secondary clock is generated from a 27 Megahertz crystal. the clock domain is generally used for internal video clock generation.

2.7 Battery

The DM355 EVM incorporates a battery holder to provide backup power to the MSP430's real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 2: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM355 EVM and its interfaces.

Topic **Page**

3.1	Board Layout	3-3
3.2	Connectors	3-5
3.2.1	J1, NTSC/PAL Select	3-6
3.2.2	J2, Video In	3-7
3.2.3	J3, MSP430 JTAG Header	3-7
3.2.4	J4, Composite Video Out	3-8
3.2.5	J5, USB Connector and Jumpers	3-8
3.2.6	J6, 14 Pin External JTAG Connector	3-9
3.2.7	J8, ARM JTAG Emulation Header	3-10
3.2.8	J9, USB Capacitance Select	3-10
3.2.9	J10, USB ID Select	3-11
3.2.10	J11, S-Video In	3-11
3.2.11	J12, ATA/CE Interface	3-12
3.2.12	J16, +5V Input	3-13
3.2.13	J27, MMC/SD Connector	3-13
3.2.14	J28, MMC/SD Connector	3-14
3.2.15	J30, Imager Interface Connector 1	3-15
3.2.16	J31, Imager Interface Connector 2	3-16
3.2.17	P1, Microphone In	3-17
3.2.18	P2, Headphone Out	3-18
3.2.19	P3, Line Out	3-18
3.2.20	P4, RS-232 UART	3-19
3.2.21	P5, Ethernet Interface	3-20
3.2.22	P6, Line In	3-21
3.2.23	DC3, I/O Daughter Card Expansion	3-22
3.2.24	DC5, TH8200 Daughter Card Interface	3-23
3.2.25	DC6, Expansion Connector	3-24
3.2.26	DC7, Expansion Connector	3-24
3.2.27	U10, Infrared Interface	3-25

Topic		Page
3.3	**LEDs**	**3-25**
3.4	**Switches**	**3-26**
3.4.1	**SW1, EMU0/1 Select Switch**	**3-26**
3.4.2	**SW5, Reset Switch**	**3-27**
3.4.3	**SW6, User Readable 4 Position DIP Switch**	**3-27**
3.4.4	**SW7, ARM Boot Mode Select**	**3-28**
3.4.5	**SW10 - SW14**	**3-28**
3.5	**Test Points**	**3-29**

3.1 Board Layout

The DM355 EVM is a 5.0 x 6.5 inch (127 x 165 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the top side of the DM355 EVM.

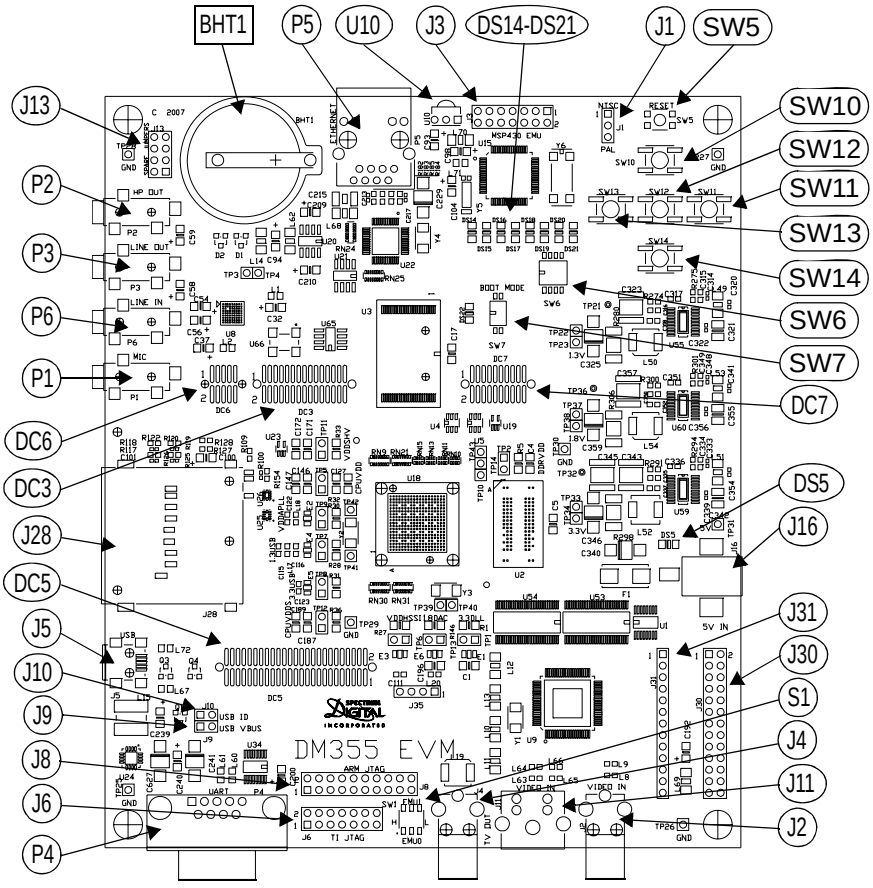


Figure 3-1, DM355 EVM, Interfaces Top Side

Figure 3-2 shows the layout of the bottom side of the DM355 EVM.

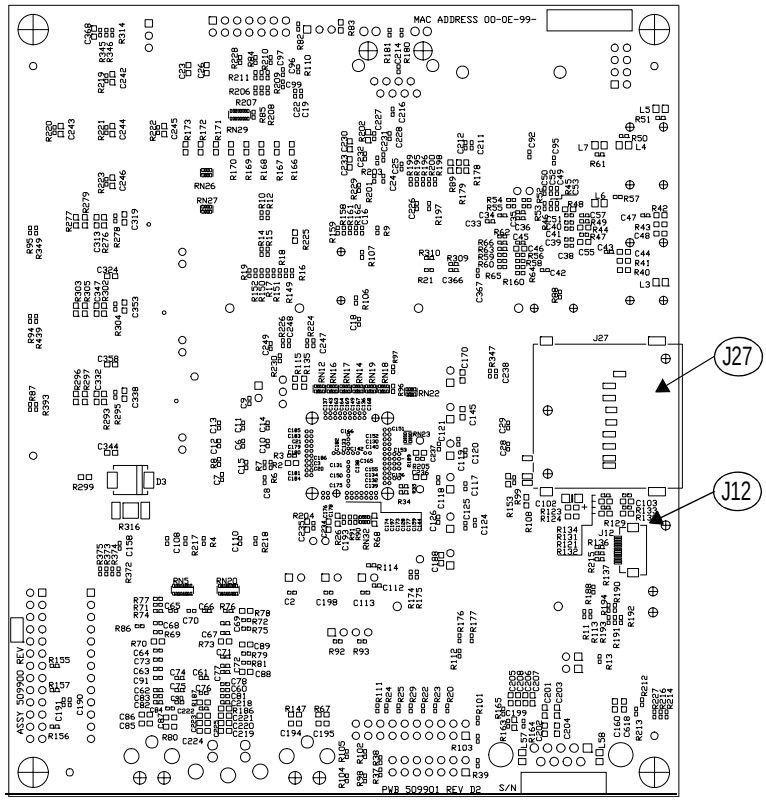


Figure 3-2, DM355 EVM, Interfaces Bottom Side

3.2 Connectors

The EVM has numerous connectors and option jumpers to control and provide connections to various peripherals. These connectors and jumpers are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J1	1 x 3	NTSC/PAL Video Select
J2		Video In
J3	2 x 7	MSP430 JTAG
J4	8	Composite Video Out
J5	1 x 4	Mini A/B USB Connector
J6	2 x 7	TI 14 Pin JTAG
J8	2 x 8	ARM JTAG Emulation Header
J9	2 x 1	USB Capacitor
J10	2 x 1	USB ID Jumper
J11	4	Video In
J12	12 x 1	ATA/CE Interface
J13	4 x 2	Spare Jumper Storage
J16	2	+5V In
J27	18	SD/MMC Connector
J28	18	SD/MMC Connector
J30	13 x 2	Imager Interface
J31	13 x 1	Imager Interface
P1	4	Microphone In
P2	2x5	Headphone Out
P3	4	Line Out
P4	9	RS-232 UART
P5	12	Ethernet
P6	4	Line In
DC3	15 x 2	I/O Daughter Card Expansion
DC5	25 x 2	THS8200 Daughter Card Interface
DC6	5 x 2	Expansion Connector
DC7	10 x 2	GP I/O Signals
U10		Infrared Receiver

3.2.1 J1, NTSC/PAL Select

The J1 connector is a 3 position jumper located on the top side of the board and is used to select the type of video data the DM355 will be working with. NTSC format is expected if the jumper is in the 1-2 position. The selection of 2-3 indicates PAL format data will be used. Either the NTSC (1-2 position) or PAL (2-3 position) **must** be selected. To reconfigure this selection, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The image of this jumper is shown in the figure below.

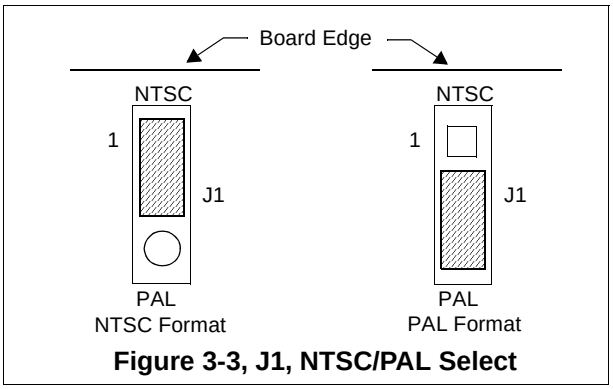


Figure 3-3, J1, NTSC/PAL Select

Table 2: J15, NTSC/PAL Select

Video Format	Position
NTSC	1-2
PAL	2-3

3.2.2 J2, Video In

J2 is an RCA jack used as a composite video input to the TVP5146 encoder. This connector brings in a video signal to pin 8 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

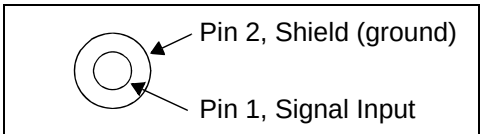


Figure 3-4, J2, Video In RCA Jack

Table 3: J2, Video In, RCA Jack

Pin #	Signal Name
1	Pin 8, TVP5146
2	GND

3.2.3 J3, MSP430 JTAG Header

The J3 MSP430 JTAG Header is located on the top side of the board and is used to provide a programming interface to the MSP430 microcontroller. The pinout for the J3 connector is shown in the table below. This connector is typically used for factory use only.

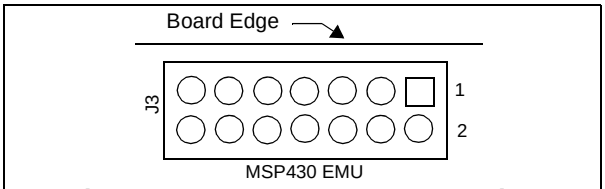


Figure 3-5, J3, MSP430 JTAG Header

Table 4: J3, MSP430 JTAG Header

Pin #	Signal	Pin #	Signal
1	430_TDO	2	NC
3	430_TDI	4	MSP430_3V3
5	430_TMS	6	NC
7	430_TCK	8	NC
9	GND	10	NC
11	430_RESET	12	NC
13	NC	14	NC

3.2.4 J4, Composite Video Out

Connector J4 is an RCA jack used as a composite video output from the “TVOUT” signal of the TMS320DM355. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

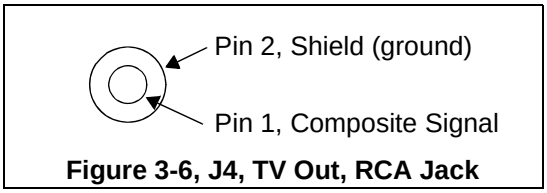


Figure 3-6, J4, TV Out, RCA Jack

Table 5: J4, TV Out, RCA Jack

Pin #	Signal Name
1	Composite video output
2	GND

3.2.5 J5, USB Connector and Jumpers

Connector J5 is a mini A/B USB connector. The pinout for the J5 connector is shown in the figure below.

Table 6: J5, USB Connector

Pins	Signal
1	USB_VBUS
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD

* Use internal register to swap DM/DP pair. This feature was used to improve printed circuit board routing.

The EVM incorporates the ability to toggle the ID pin on the USB connector via software control. The GIO2 pin on the DM355 controls this function.

For “USB ON The Go” mode remove jumper J10. This will allow the cable to configure the ID pin on the DM355 processor.

The EVM supplies up to 500 ma of current to the USB_VBUS via a TPS61092 DC/DC converter. This is enabled via the DM355’s DRV_VBUS pin. J9 supplies extra capacitance for host mode operations. Remove J9 for “USB On The Go” operations. Spare jumpers can be stored on connector J13.

3.2.6 J6, 14 Pin External JTAG Connector

Connector J6 is a 2 x7 double row male header with pin 6 clipped to serve as a key. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure below.

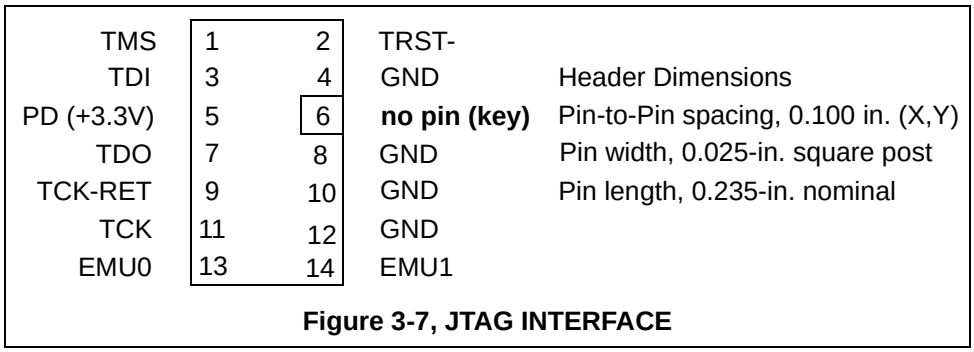


Figure 3-7, JTAG INTERFACE

The signal names for each pin are shown in the table below.

Table 7: J6, JTAG Interface

Pin #	Signal Name	Pin #	Signal Name
1	TMS	2	TRST-
3	TDI	4	GND
5	PD	6	no pin - key
7	TDO	8	GND
9	TCKRET	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

* **Note:** EMU0/EMU1 mode must be selected to ICEPICK mode

3.2.7 J8, ARM JTAG Emulation Header

The J8 Emulation Header is located on the top side of the board and is used to provide an interface to ARM compatible JTAG emulators. The pinout for this connector is shown in the table below.

Table 8: J8, ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

* **Note:** EMU0/EMU1 switch must be set to ARM mode

3.2.8 J9, USB Capacitance Select

The J9 jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

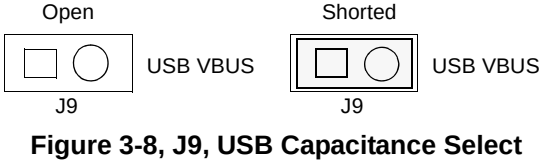


Figure 3-8, J9, USB Capacitance Select

Table 9: J9, USB Capacitance Select

Position	Function
Open	6.9 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.9 J10, USB ID Select

The J10 jumper is used to allow the cable to configure the ID pin on the DM355. This is used for the “USB On The Go” mode. When the jumper is shorted, access to the ID is provided. The open and shorted position are shown below.

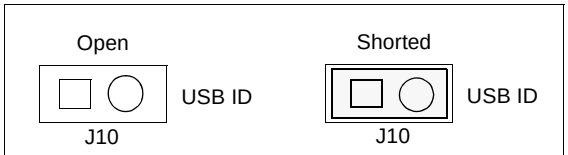


Figure 3-9, J10, USB ID Select

Table 10: J10, USB ID Select

Position	Function
Open	ID from USB connector
Shorted	ID controlled from GIO2

3.2.10 J11, S-Video In

Connector J11 is a four pin mini din connector which interfaces to the TVP5146 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

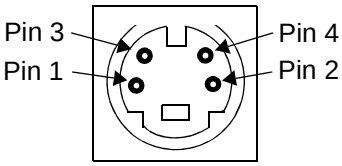


Figure 3-10, J11, Front View, Mini Din Connector

Table 11: J11, Video In, Mini Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

3.2.11 J12, ATA/CE Interface

Connector J12 is a 12 x 1 flex cable connector mounted on the bottom side of the board. The signals on this connector parallel the signals present on the connector J28 which is located on the top side of the board. The signals present on connector J12 are shown in the table below. when this connector is used the corresponding SD connector can not be used.

Table 12: J12, ATA/CE Interface

Pin #	Signal Name
1	Ground
2	SD1_DAT2
3	SD1_DAT3
4	VCC_3V3
5	SD1_CMD
6	VCC_3V3
7	SD1_CLK
8	Ground
9	SD1_DATA0
10	SD1_DATA1
11	Ground
12	NC

3.2.12 J16, +5V Input

Connector J16 is the input power connector. This connector bring in +5 volts to the EVM. This is a 2.5mm. jack. Inside of the jack is tied to through a fuse to VCC_5V. The other side is tied to ground and LED DS5. The figure below shows this connector as viewed from the card edge.

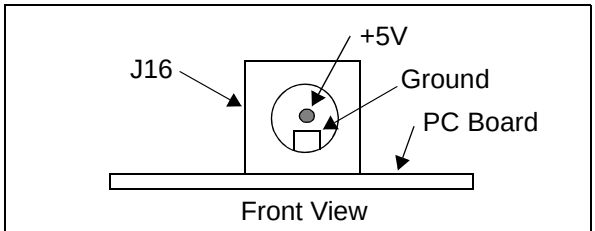


Figure 3-11, J16, +5 Volt Input Connector

3.2.13 J27, MMC/SD Connector

The J27 MMC/SD connector is located on the bottom side of the board and is used to provide an interface to a MMC/SD card. The pinout for the J27 connector is shown in the table below.

Table 13: J27, MMC/SD Connector

Pin #	Signal	Pin #	Signal
1	SD0_DATA3	2	SD0_CMD
3	GND	4	VCC_3V3
5	SD0_CLK	6	GND
7	SD0_DATA0	8	SD0_DATA1
9	SD0_DATA2	10	Write Protect 0
11	GND	12	Insert 0

3.2.14 J28, MMC/SD Connector

The J28 MMC/SD connector is located on the top side of the board and is used to provide an interface to a MMC/SD card. The signals present on J28 are also present on J12. Therefore, when J28 is used the operator can not use J12 for a CE-ATA disk drive. The pinout for the J28 connector is shown in the table below.

Table 14: J28, MMC/SD Connector

Pin #	Signal	Pin #	Signal
1	SD1_DATA3	2	SD1_CMD
3	GND	4	VCC_3V3
5	SD1_CLK	6	GND
7	SD1_DATA0	8	SD1_DATA1
9	SD1_DATA2	10	Write Protect 1
11	GND	12	Insert 1

3.2.15 J30, Imager Interface Connector 1

The connector J30 is a 13 x 2 double row header which is part of the imager interface. It is used with connector J31. The pinout for the J30 connector is shown in the table below.

Table 15: J30, Imager Interface Connector 1

Pin #	Signal	Pin #	Signal
1	IMAGER_D4	2	IMAGER_D5
3	IMAGER_D6	4	IMAGER_D7
5	IMAGER_D8	6	IMAGER_D9
7	IMAGER_D10	8	IMAGER_D11
9	IMAGER_D2	10	IMAGER_D3
11	Ground	12	Ground
13	IMAGER_LINE_VALID	14	NC
15	NC	16	IMAGER_RESET
17	IMAGER_FRAME_VALID	18	I2C_DATA_IMG
19	I2C_SCLK_IMG	20	NC
21	IMAGER_VBUS	22	IMAGER_VBUS
23	IMAGER_PXCLK	24	Ground
25	Ground	26	Ground

Note: When using the imager the user needs to select the video input multiplier to imager mode via I^2C control registers in the MSP430.

3.2.16 J31, Imager Interface Connector 2

The connector J31 is a 13 x 1 single row header which is part of the imager interface. It is used with connector J30. The pinout for the J31 connector is shown in the table below.

Table 16: J30, Imager Interface Connector 1

Pin #	Signal
1	IMAGER_D0
2	IMAGER_D1
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	IMAGER_GBL_SHUTTER
11	IMAGER_TRG
12	NC
13	Ground

Note: When using the imager the user needs to select the video input multiplier to imager mode via I^2C control registers in the MSP430.

3.2.17 P1, Microphone In

The microphone input, P1 is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signal is connected to signals “MIC3R” and “MIC3L” of the AIC33. The signals on the plug are shown in the figure below.

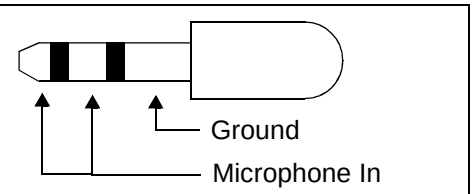


Figure 3-13, Microphone Input Jack

3.2.18 P2, Headphone Out

The P2 connector is a 3.5 mm. stereo headphone output from the TVL320AIC33 on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

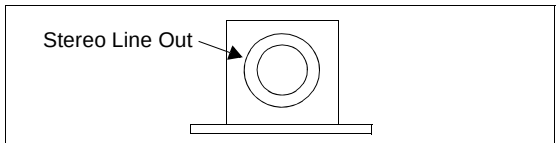


Figure 3-14, P2, Headphone Out Interface

Table 17: P2, Headphone Out Interface

Pin #	AIC33 Signal
1	Ground
2	HPLOUT
3	HPROUT
4	NC

3.2.19 P3, Line Out

The audio line out connector P3, is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

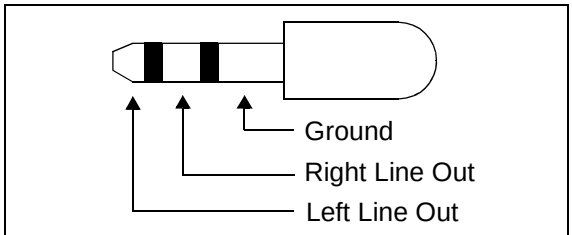


Figure 3-15, Audio Line Out Stereo Jack

Table 18: P3, Audio Line Out Stereo Jack

Pin #	AIC33 Signal
1	Ground
2	LEFT_LO+
3	RIGHT_LO+
4	NC

3.2.20 P4, RS-232 UART

The P4 connector is a 9 pin make D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U34) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

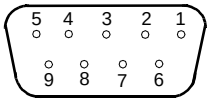


Figure 3-16, P4, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 19: P4, RS-232 Pinout

Pin #	Signal Name
1	NC
2	DM355 UART0 Rx Data
3	DM355 UART0 Tx Data
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.3.21 P5, Ethernet Interface

The P5 connector is located on the top side of the board and is used to provide an Ethernet interface. P5 integrates the magnetics and standard RJ-45 connector. The two tables below shoe the signals present on the magnetics interface and the connector side.

Table 20: P5, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	ENET_TXO+	2	ENET_TXO-
3	ENET_RXI+	4	ENET_2V5(RX Center Tap)
5	ENET_2V5(RX Center Tap)	6	ENET_RXI-
7	NC	8	GND
9	VCC_3V3(LED1+)	10	ENET_LED1(LED1-)
11	VCC_3V3(LED2+)	12	ENET_LED2(LED2-)

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 21: P5, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TX_DATA+	2	TX_DATA-
3	RX_DATA+	4	NC
5	NC	6	RX_DATA-
7	NC	8	NC

3.2.22 P6, Line In

Connector P6 is an stereo audio line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

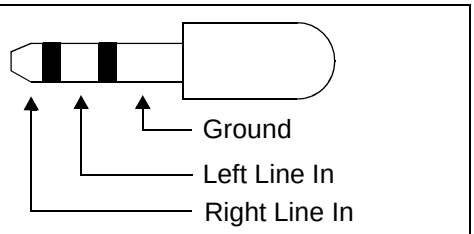


Figure 3-17, P6, Audio Line In Stereo Jack

Table 22: P6, Headphone Out Interface

Pin #	AIC33 Signal
1	Ground
2	LINE2L+
3	LINE2R+
4	NC

3.2.23 DC3, I/O Daughter Card Expansion

The DC3 connector is an I/O expansion interface for a daughter card. This is a 15 x 2 pinned female surface mount connector. The pinout for the DC3 connector is shown in the table below.

Table 23: DC3, I/O Daughter Card Expansion

Pin #	Signal	Pin #	Signal
1	SPI1_SDENA0	2	NC
3	SPI1_SDI	4	SPI_SDO
5	SPI1_CLK	6	DM355_TIMERIN3
7	Ground	8	Ground
9	McBSP_DR0	10	McBSP_DX0
11	McBSP_CLKR0	12	McBSP_CLKX0
13	McBSP_FSR0	14	McBSP_FSX0
15	Ground	16	Ground
17	SYS_RESETz	18	I2C_SCLK
19	UART1_TXD	20	I2C_DATA
21	UART1_RXD	22	Ground
23	Ground	24	GIO18
25	VCC_3V3	26	VCC_3V3
27	Ground	28	Ground
29	VCC_5V	30	VCC_5V

The manufacturer and part number of this connector is: SAMTEC SFM-115-02-S-D-LC

A possible mating connector is: SAMTEC TFM-115-32-S-D-LC. This height is .44 inches. Your actual height may vary.

3.2.24 DC5, TH8200 Daughter Card Interface

The DC5 connector is an expansion interface for the TH8200 daughter card. This is a 25 x 2 pinned female surface mount connector. The pinout for the DC5 connector is shown in the table below.

Table 24: DC5, TH8200 Daughter Card Interface

Pin #	Signal	Pin #	Signal
1	VDOUT_LCD_OE	2	GIO16
3	VDOUT_FIELD	4	GIO17
5	DM355_GIO6	6	DM355_GIO7
7	Ground	8	Ground
9	VDOUT_C0	10	VDOUT_C1
11	VDOUT_C2	12	VDOUT_C3
13	VDOUT_C4	14	VDOUT_C5
15	VDOUT_C6	16	VDOUT_C7
17	Ground	18	Ground
19	VDOUT_EXTCLK	20	CDOUT_HSYNC
21	Ground	22	Ground
23	VDOUT_VCLK	24	CDOUT_VSYNC
25	Ground	26	Ground
27	VDOUT_Y0	28	VDOUT_Y1
29	VDOUT_Y2	30	VDOUT_Y3
31	VDOUT_Y4	32	VDOUT_Y5
33	VDOUT_Y6	34	VDOUT_Y7
35	Ground	36	Ground
37	I2C_SCLK	38	DC5_RESETn
39	I2C_DATA	40	Ground
41	VCC_1V8	42	VCC_1V8
43	Ground	44	Ground
45	VCC_3V3	46	VCC_3V3
47	Ground	48	Ground
49	VCC_5V	50	VCC_5V

The manufacturer and part number of this connector is: SAMTEC SFM-125-02-S-D-LC

A possible mating connector is: SAMTEC TFM-125-32-S-D-LC. This height is .44 inches. Your actual height may vary.

3.2.25 DC6, Expansion Connector

The DC6 connector is an expansion connector used to provide compatibility with the THS8200 video daughter card. This is a 5 x 2 pinned female surface mount connector. The pinout for the DC6 connector is shown in the table below.

Table 25: DC6, Video Output Connector

Pin #	Signal	Pin #	Signal
1	NC	2	NC
3	VCC_3V3	4	Ground
5	NC	6	NC
7	NC	8	NC
9	Ground	10	Ground

The manufacturer and part number of this connector is: SAMTEC SFM-105-02-S-D-LC

A possible mating connector is: SAMTEC TFM-105-32-S-D-LC. This height is .44 inches. Your actual height may vary.

3.2.26 DC7, Expansion Connector

Extra EMIF signals are available as general purpose I/O in some configurations. Connector DC7 provides access to these pins. This is a 10 x 2 pinned female surface mount connector. The pinout for the DC7 connector is shown in the table below.

Table 26: DC7, Expansion Connector

Pin #	Signal	Pin #	Signal
1	GIO54	2	GIO67
3	GIO65	4	GIO31
5	GIO63	6	GIO64
7	Ground	8	Ground
9	GIO62	10	GIO61
11	GIO60	12	GIO59
13	GIO58	14	GIO57
15	GIO56	16	GIO032
17	Ground	18	Ground
19	VCC_3V3	20	VCC_3V3

3.2.27 U10, Infrared Interface

U10 is an infrared receiver mounted on the edge of the board. This device interfaces to the MSP430 mircrocontroller. The view of U10 is shown from a board edge view in the figure below.

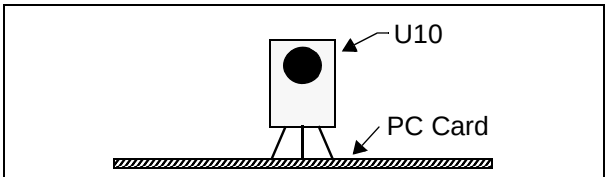


Figure 3-18, U10, IR Interface, Card Edge View

The receiver supports interaction with an Infrared remote control included with your EVM

3.3 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Information regarding the LEDs are shown in the table below.

Table 27: LEDs

LED #	Use	Color
DS5	+5 Volts present	Green
DS14	User control via MSP430 I^2C	Green
DS15	User control via MSP430 I^2C	Green
DS16	User control via MSP430 I^2C	Green
DS17	User control via MSP430 I^2C	Green
DS18	User control via MSP430 I^2C	Green
DS19	User control via MSP430 I^2C	Green
DS20	User control via MSP430 I^2C	Green
DS21	User control via MSP430 I^2C	Green
DS22	Boot Mode Status	Green

3.4 Switches

The EVM has nine (9) switches. The function of these switches are shown in the table below.

Table 28: Switches

Switch	Function	Type
SW1	EMU0/EMU1 Control	4 Position DIP
SW5	Reset	Push Button/Momentary
SW6	User Readable	4 Position DIP
SW7	ARM Boot Mode Select	2 Position DIP
SW10	User Readable	Push Button/Momentary
SW11	User Readable	Push Button/Momentary
SW12	User Readable	Push Button/Momentary
SW13	User Readable	Push Button/Momentary
SW14	User Readable	Push Button/Momentary

3.4.1 SW1, EMU0/1 Select Switch

SW1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the TMS320DM355 processor. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

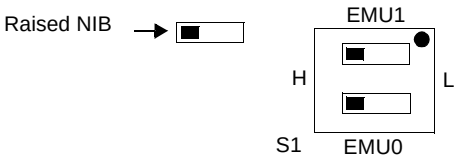


Figure 3-19, SW1, EMU0/1 Select Switch

Table 29: SW1, EMU0/1 Select

State at Reset EMU1	State at Reset EMU0	Function
L(0)	L(0)	Emulation Debug ARM JTAG Enabled
L(0)	H(1)	Not Defined
H(1)	L(0)	Not Defined
H(1)	H(1)	ICE PICK Mode * Both ARM & DSP JTAG Enabled

* is the factory shipped configuration

3.4.2 SW5, Reset Switch

Switch SW5 is a push button reset switch that will RESET the board. The MSP430 controls all reset and power monitoring logic on the EVM.

3.4.3 SW6, User Readable 4 Position DIP Switch

Switch SW6 is a 4 position DIP switch with each position being an input to the MSP430 microcontroller and accessible to the DM355 via the I^2C control registers. The table below shows what signal each position appears on.

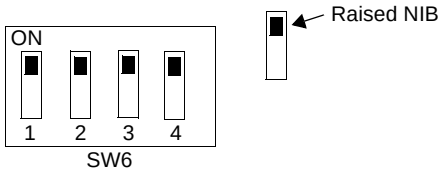


Figure 3-20, SW6, User Readable 4 Position DIP Switch

.

Table 30: SW6, User Readable 4 Position DIP Switch

Position	Signal
1	SW_DIP0
2	SW_DIP1
3	SW_DIP2
4	SW_DIP3

3.4.4 SW7, ARM Boot Mode Select

Switch SW7 is a 2 position DIP switch used to select the ARM Boot Mode. The figure and table below show these options.

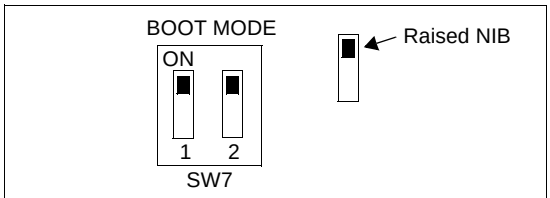


Figure 3-21, SW7, ARM Boot Mode Select

Table 31: SW7, ARM Boot Mode Select

Pos 2	Pos 1	HW Code	Function
ON	ON	0 0	NAND boot CE0 *
ON	OFF	0 1	NOR direct execute
OFF	ON	1 0	Boot from SD/MMC
OFF	OFF	1 1	Boot from UART

***** default setting

3.4.5 SW10 - SW14

Switches S10 through SW14 are push button momentary switches that are inputs in to the MSP430 microcontroller and accessible to the DM355 via I^2C control registers on the MSP430. The table below shows what signal each switch appears on.

Table 32: SW10 - SW14, Processor Configuration/Boot Load Options

Switch	Signal
SW10	PB_SW10
SW11	PB_SW11
SW12	PB_SW12
SW13	PB_SW13
SW14	PB_SW14

3.5 Test Points

The EVM has 35 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

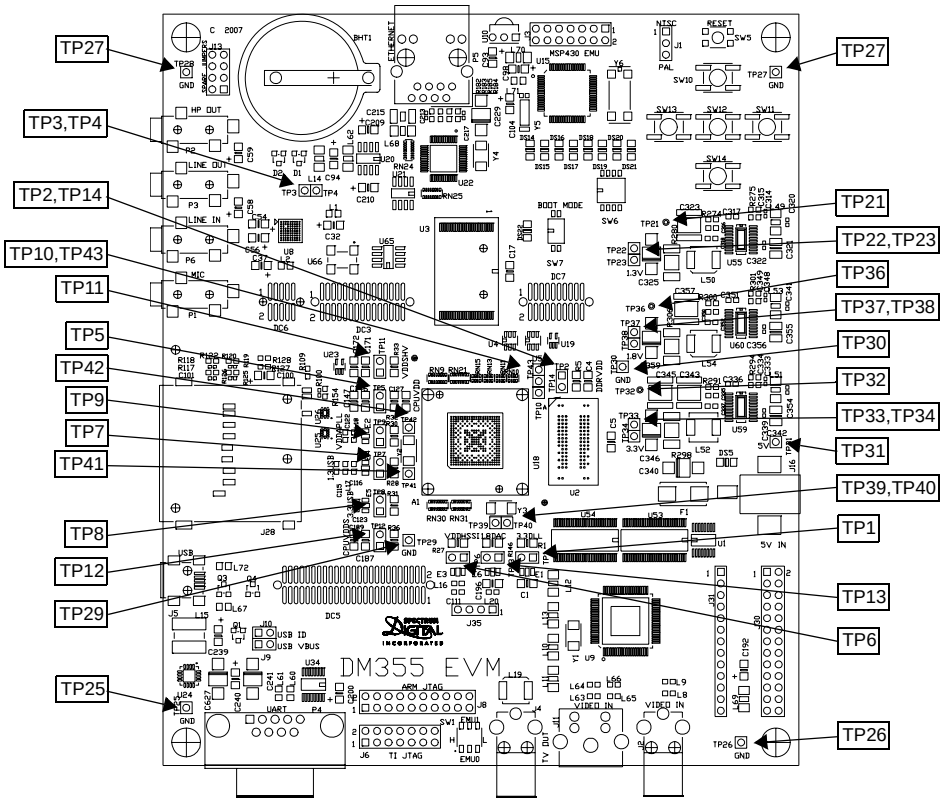


Figure 3-22, DM355 EVM, Test Points

Table 33: DM355 EVM Test Points

Test Point #	Signal	Test Point #	Signal
TP2	VCC_1V8	TP29	Ground
TP3	AIC33 MFP2	TP30	Ground
TP4	AIC33 MFP3	TP31	VCC_5V
TP10	EM_ADV/GIO032	TP32	3V3_PWR_OK
TP13	VDDA_DAC	TP33	VCC_3V3
TP14	EM_CLK/GIO031	TP36	1V8_PWR_OK
TP21	CORE_PWR_OK	TP37	VCC_1V8
TP23	VCC_1V3	TP39	TMS320DM355 MXI2
TP25	Ground	TP40	TMS320DM355 MXO2
TP26	Ground	TP41	TMS320DM355 MXI1
TP27	Ground	TP42	TMS320DM355 MXO1
TP28	Ground	TP43	EM_A7

There are 12 power test points on the EVM. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

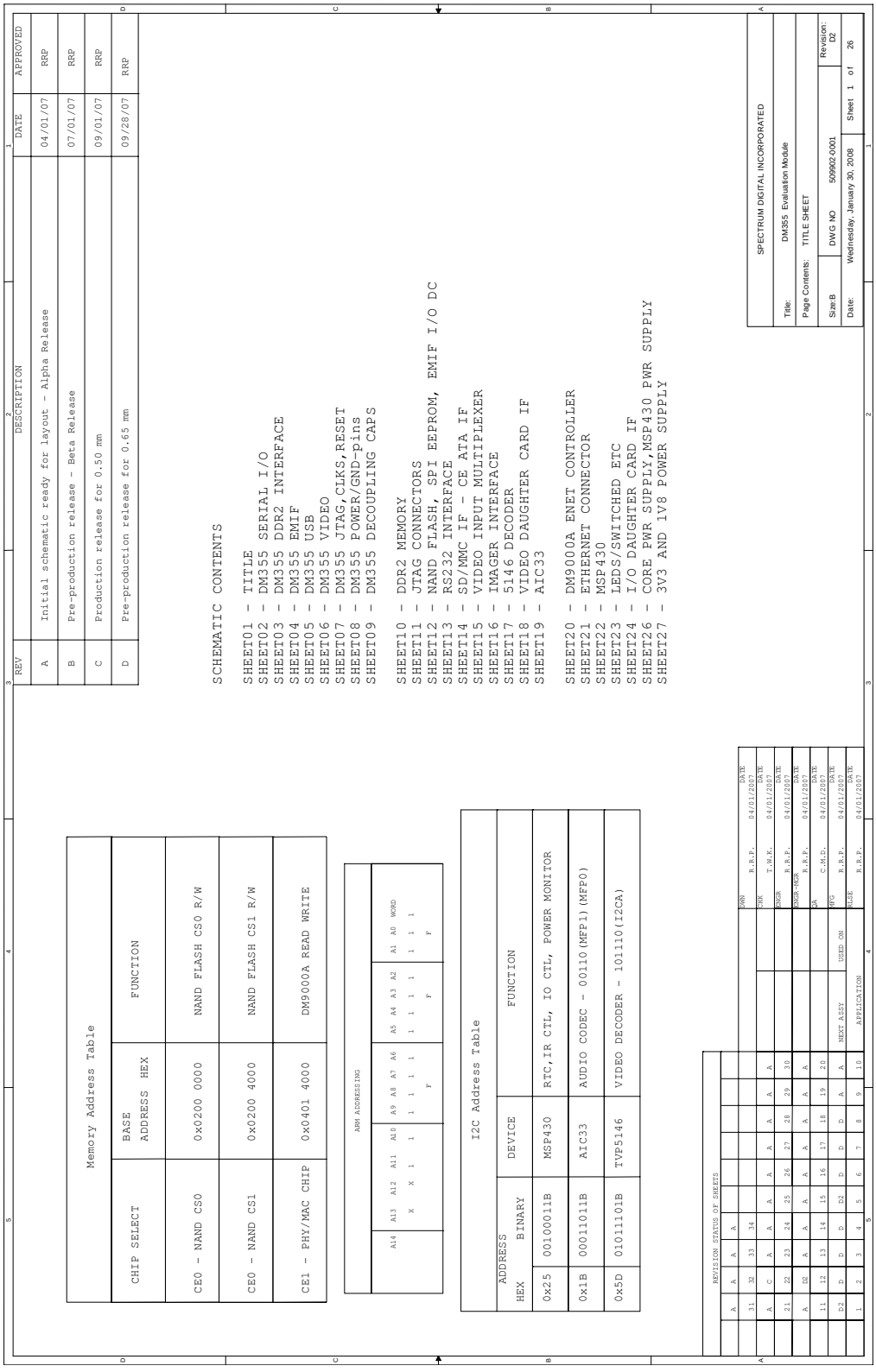
Table 34: Power Test Points

Access Test Point	Voltage	Shunt	Power Domain
TP1	+1.8V	0.02 ohms	VDDAHV3V3
TP5	+1.3V	0.02 ohms	CVDD
TP6	+1.8V	0.02 ohms	VDDA1V8 HSSI
TP7	+1.3V	0.02 ohms	USB1V3
TP8	+3.3V	0.02 ohms	USB3V3
TP9	+1.3V	0.02 ohms	VDDA.PLL1 & 2
TP11	+3.3V	0.02 ohms	VDD
TP12	+1.8V	0.02 ohms	VDDS
TP22	+1.3V	0.02 ohms	Main 1.3V
TP34	+3.3V	0.025 ohms	Main 3.3V
TP38	+1.8V	0.025 ohms	Main 1.8V
TP12	+1.8V	0.025 ohms	DDR2 Power

Appendix A

Schematics

This appendix contains the schematics for the DM355 EVM.



REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	04/01/07	RRP
B	Pre-production release - Beta Release	07/01/07	RRP
C	Production release for 0.50 mm	09/01/07	RRP
D	Pre-production release for 0.65 mm	09/28/07	RRP

SCHEMATIC CONTENTS

SHEET01 - TITLE
SHEET02 - DM355 SERIAL I/O
SHEET03 - DM355 DDR2 INTERFACE
SHEET04 - DM355 EMIF
SHEET05 - DM355 USB
SHEET06 - DM355 VIDEO
SHEET07 - DM355 JTAG,CLKS,RESET
SHEET08 - DM355 POWER/GND-pins
SHEET09 - DM355 DECOUPLING CAPS

SHEET10 - DDR2 MEMORY
SHEET11 - JTAG CONNECTORS
SHEET12 - NAND FLASH, SPI EEPROM, EMIF I/O DC
SHEET13 - RS232 INTERFACE
SHEET14 - SD/MMC IF - CE ATA IF
SHEET15 - VIDEO INPUT MULTIPLEXER
SHEET16 - IMAGER INTERFACE
SHEET17 - 5146 DECODER
SHEET18 - VIDEO DAUGHTER CARD IF
SHEET19 - AIC33

SHEET20 - DM9000A ENET CONTROLLER
SHEET21 - ETHERNET CONNECTOR
SHEET22 - MSP430
SHEET23 - LEDS/SWITCHED ETC
SHEET24 - I/O DAUGHTER CARD IF
SHEET26 - CORE PWR SUPPLY,MSP430 PWR SUPPLY
SHEET27 - 3V3 AND 1V8 POWER SUPPLY

Memory Address Table

CHIP SELECT	BASE ADDRESS HEX	FUNCTION
CE0 - NAND CS0	0x0200 0000	NAND FLASH CS0 R/W
CE0 - NAND CS1	0x0200 4000	NAND FLASH CS1 R/W
CE1 - PHY/MAC CHIP	0x0401 4000	DM9000A READ WRITE

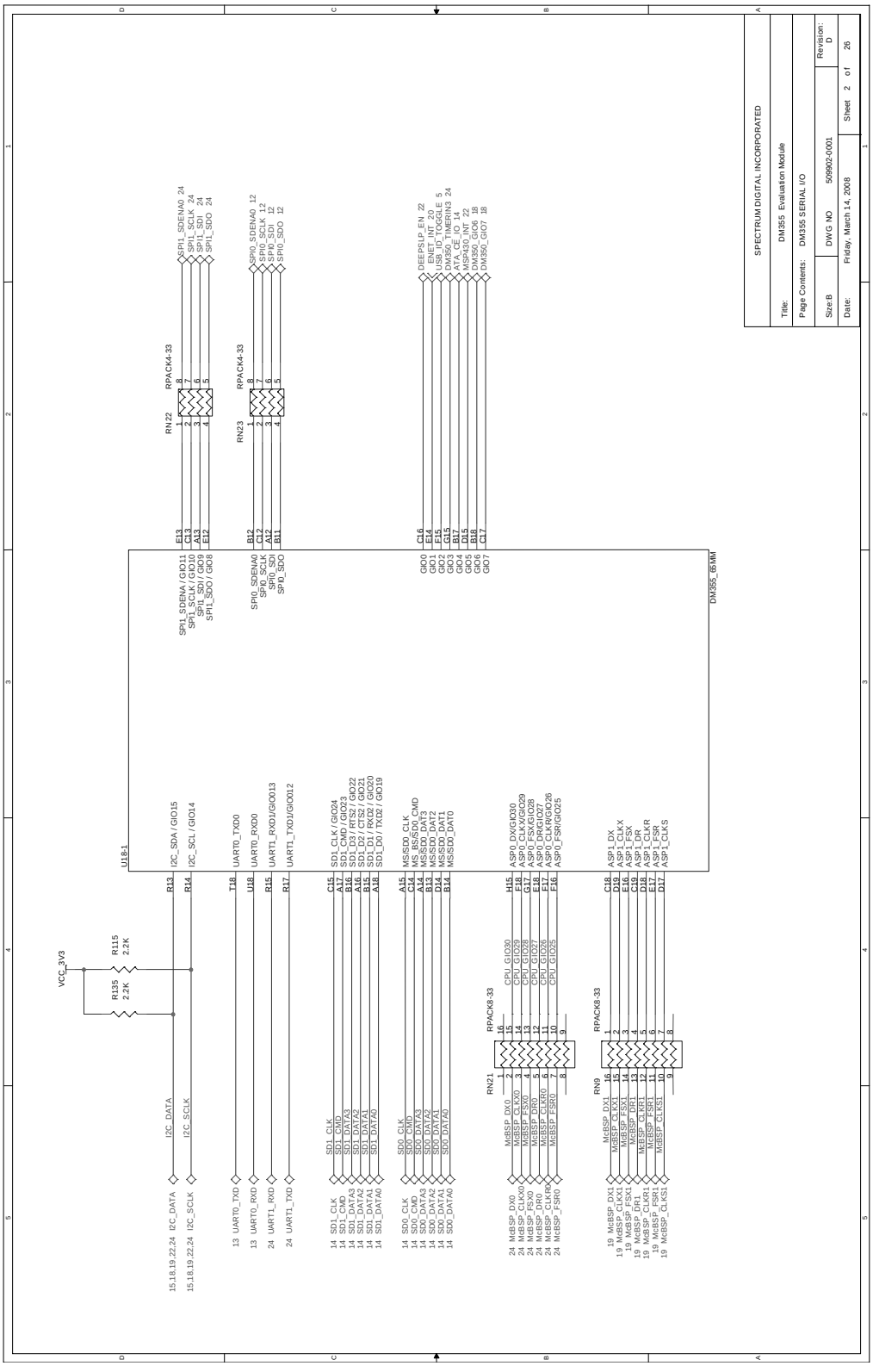
ARM ADDRESSING

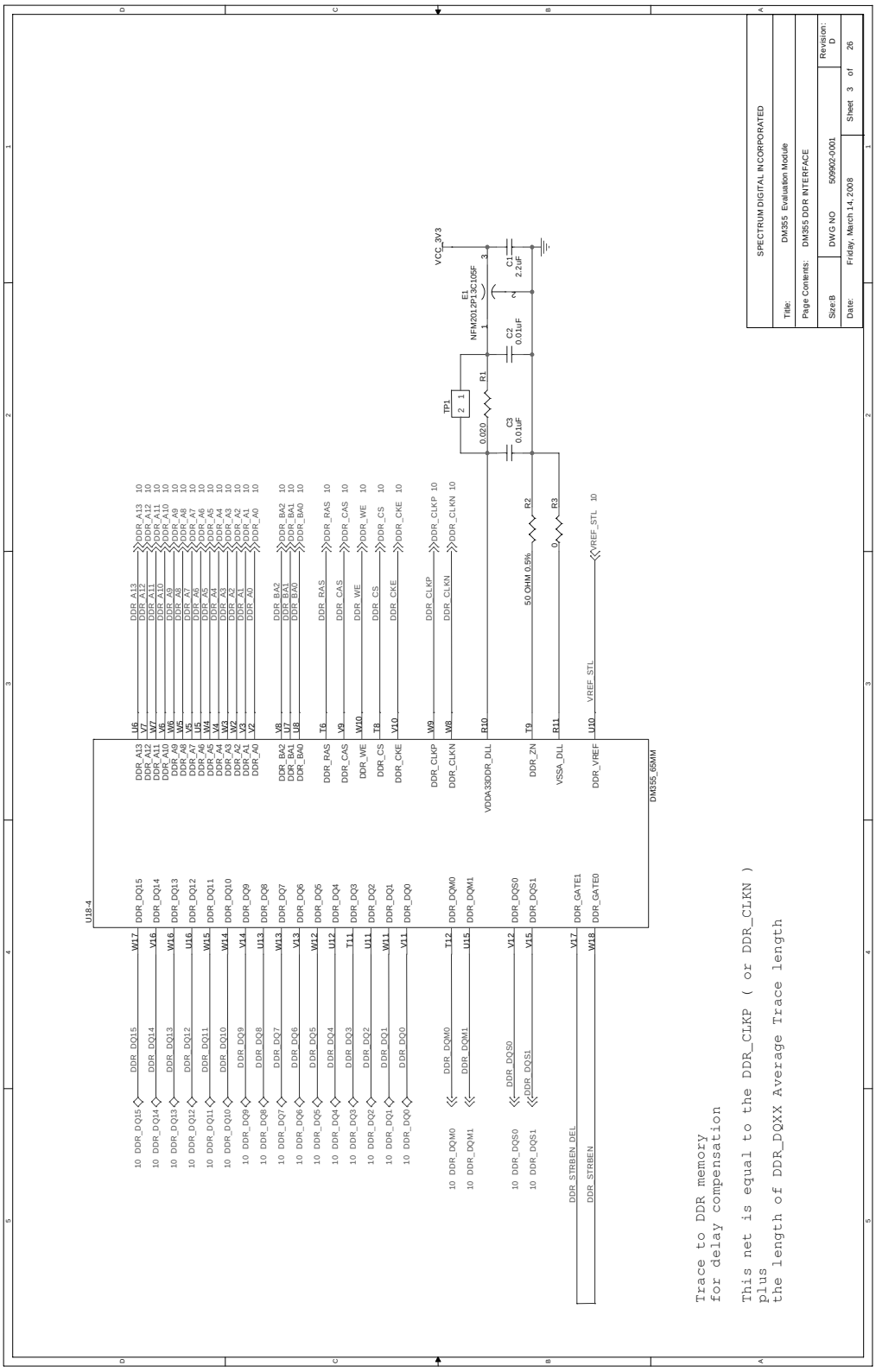
A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	WORD
	X	X	1	1	1	1	1	1	1	1	1	1	1	1	
						F					F			F	

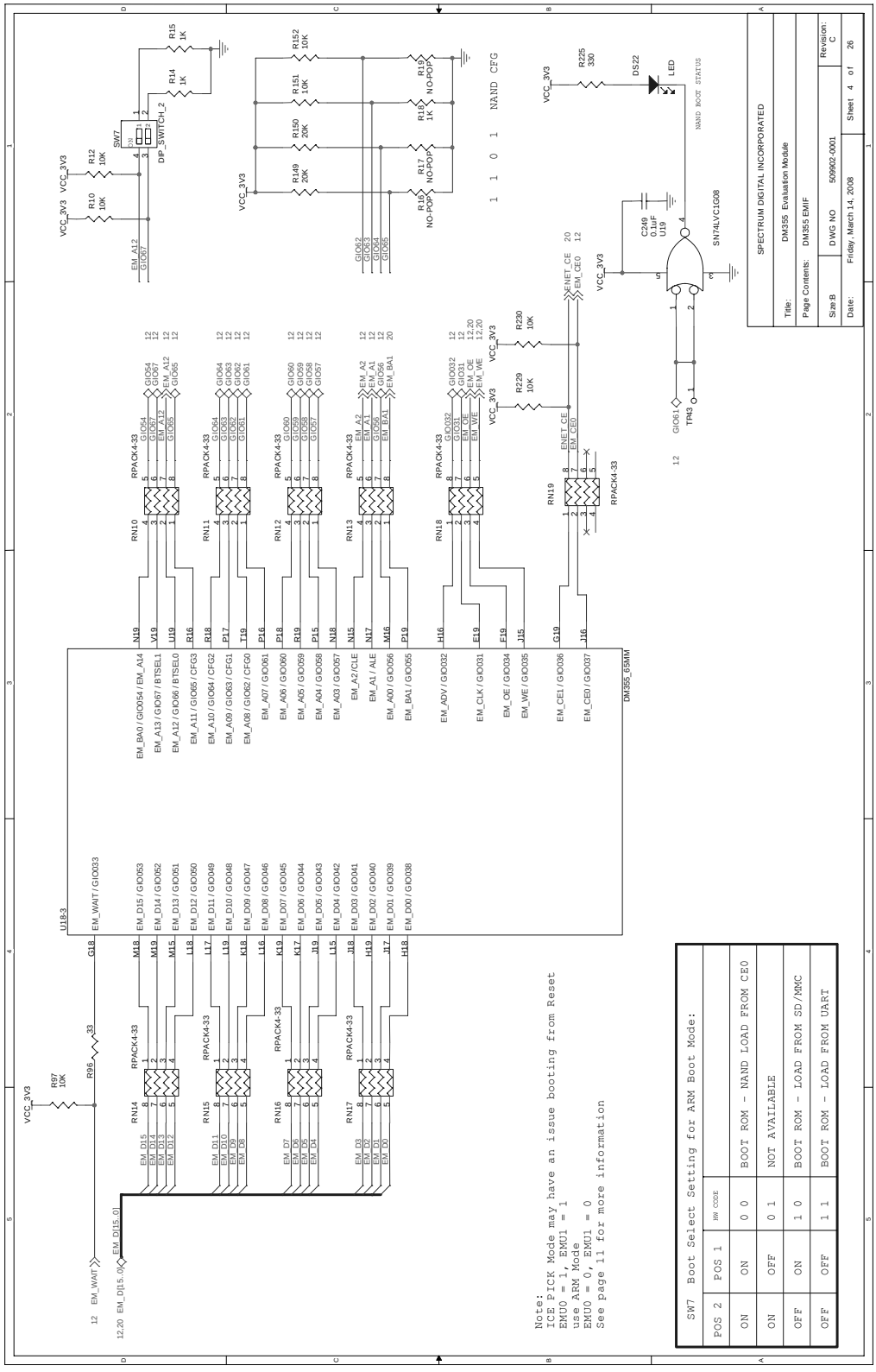
I2C Address Table

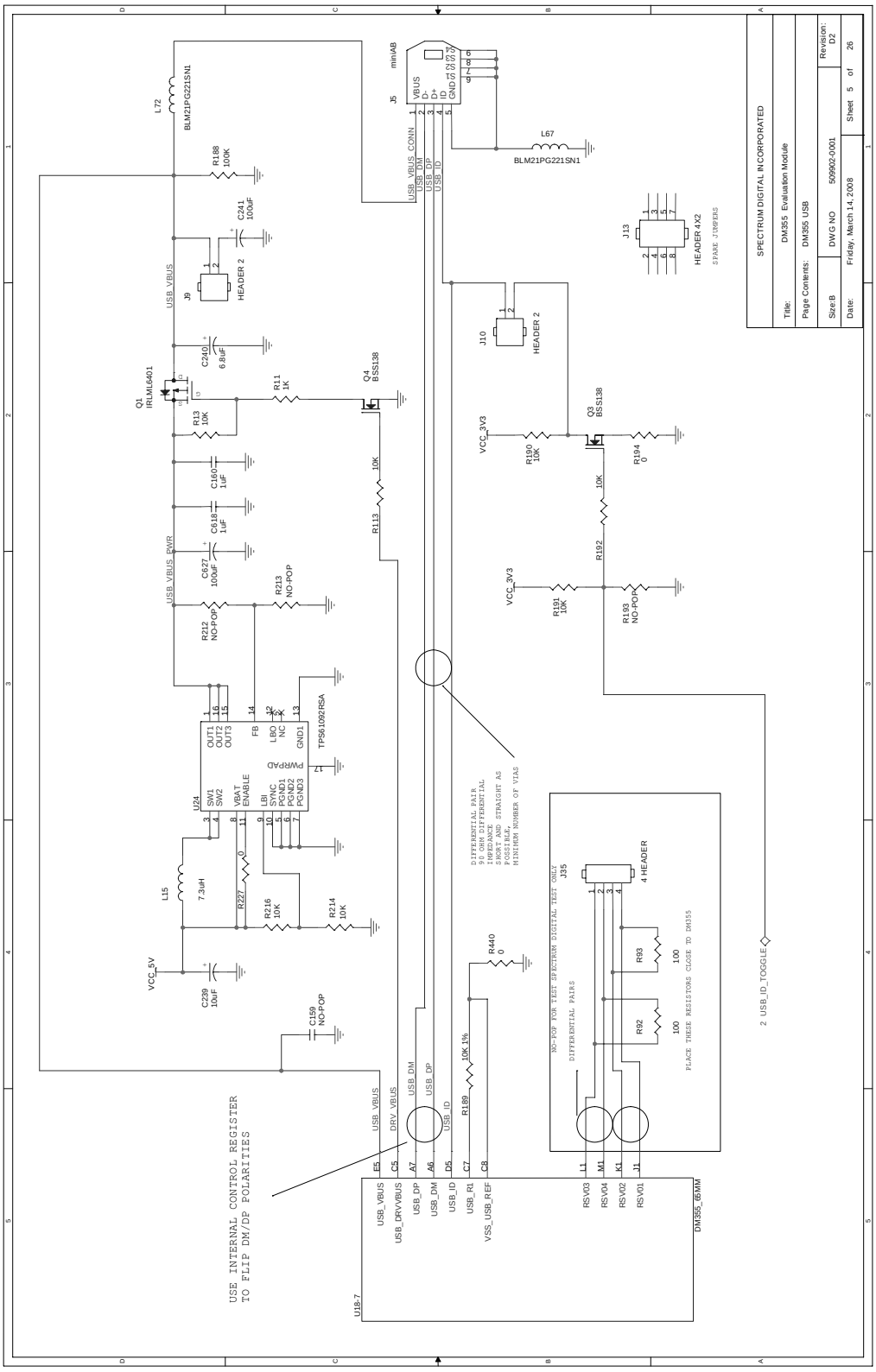
ADDRESS HEX	ADDRESS BINARY	DEVICE	FUNCTION
0x25	00100011B	MSP430	RTC,IR CTL, IO CTL, POWER MONITOR
0x1B	00011011B	AIC33	AUDIO CODEC - 00110(MFP1)(MFP0)
0x5D	01011101B	TVP5146	VIDEO DECODER - 101110(I2CA)

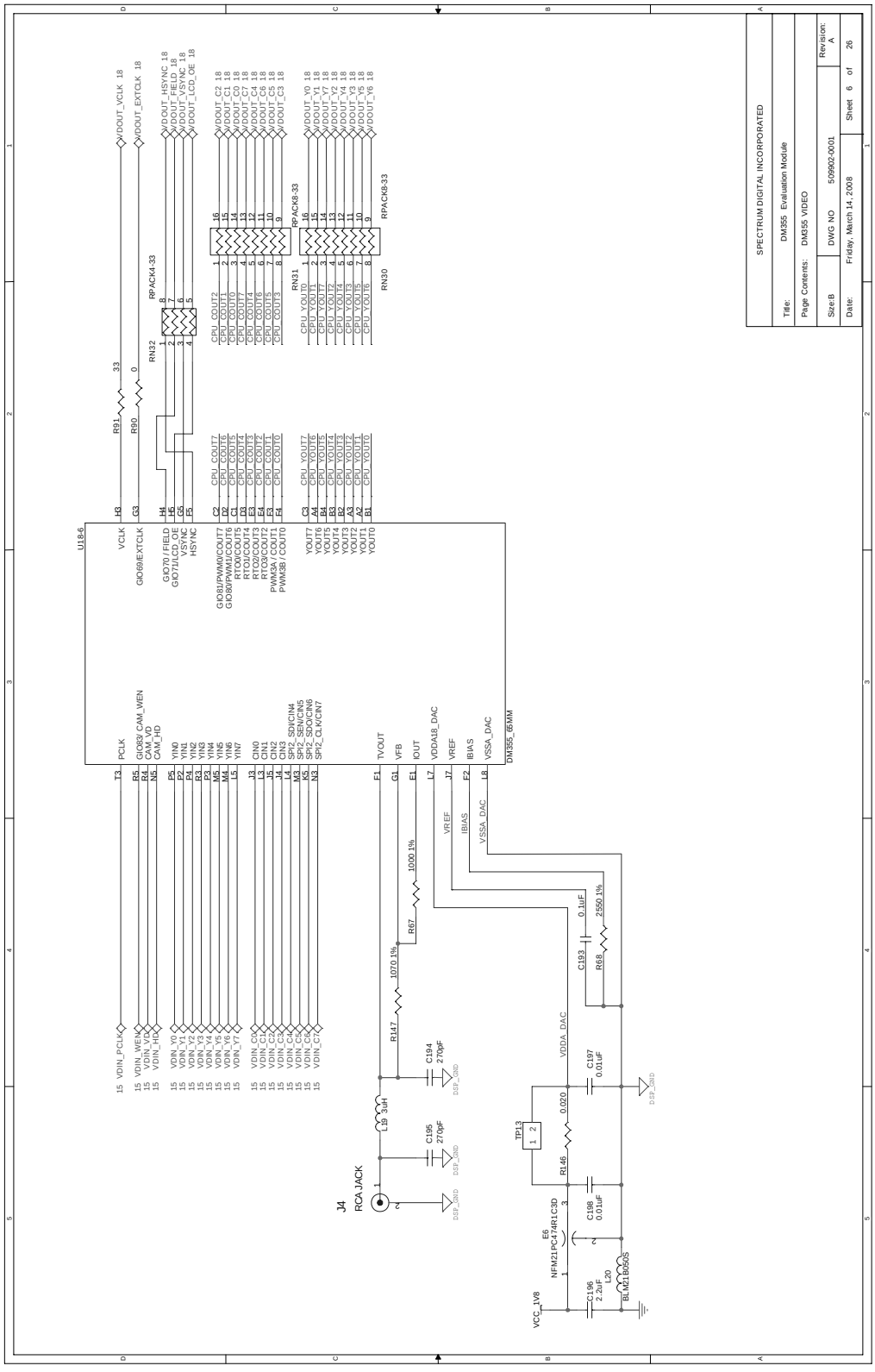
SPECTRUM DIGITAL INCORPORATED			
Title:	DM355 Evaluation Module		
Page Contents:	TITLE SHEET		
Size:B	DWG NO 505902-0001		Revision: D2
Date:	Wednesday, January 30, 2008	Sheet 1 of 26	

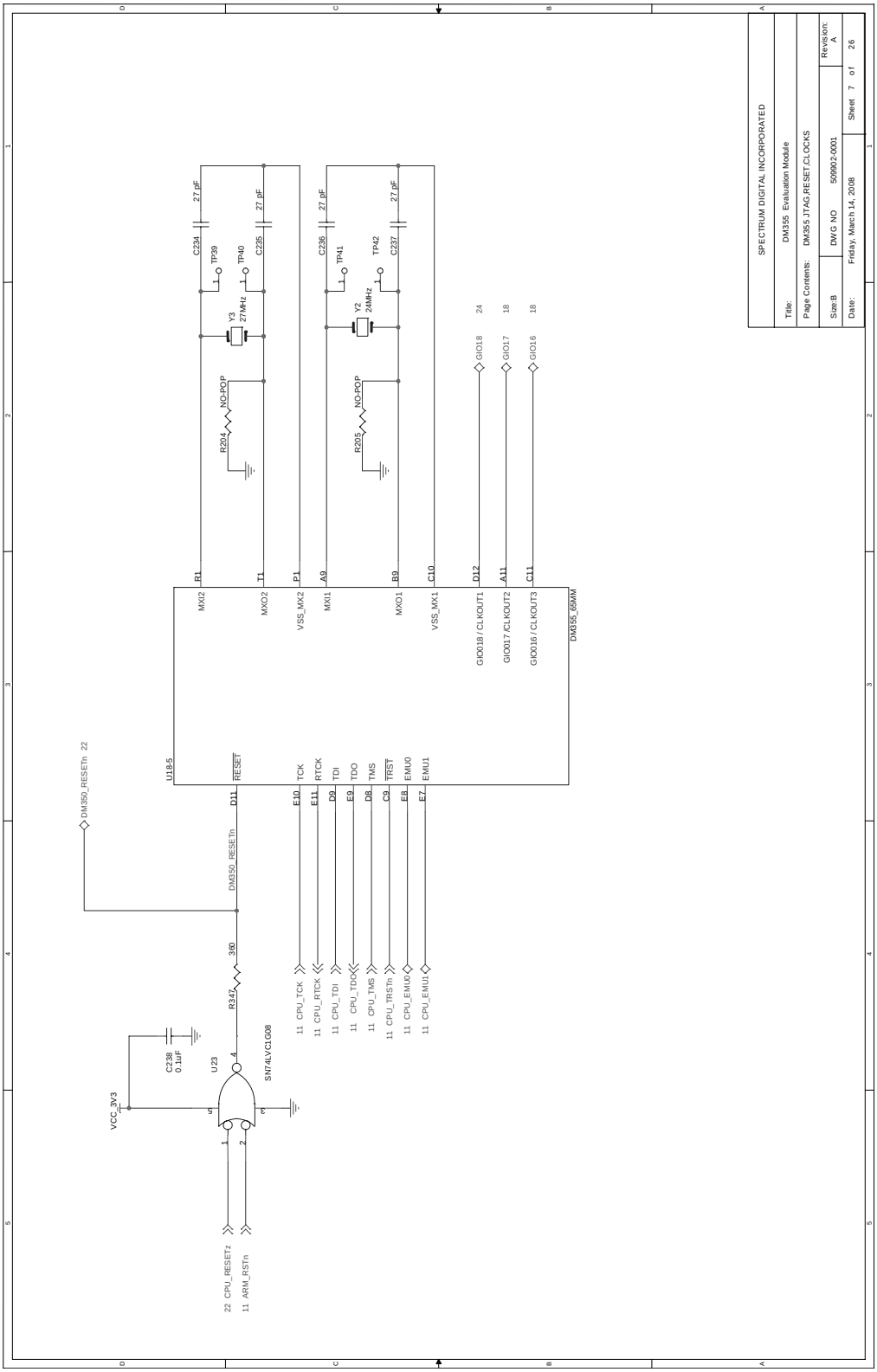

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 SERIAL I/O
Size:B
DWG NO 509902-0001
Revision: D
Date: Friday, March 14, 2008
Sheet 2 of 26
U18-1
DM355_65MM
RN22
RN23
RN21
RN9
RPACK4-33
RPACK8-33
VCC_3V3
R115 2.2K
R135 2.2K
I2C_SDA / GIO15
I2C_SCL / GIO14
UART0_TXD0
UART0_RXD0
UART1_RXD / GIO13
UART1_TXD / GIO12
SPI1_SDENA / GIO11
SPI1_SCLK / GIO10
SPI1_SDI / GIO9
SPI1_SDO / GIO8
SPI0_SDENA0
SPI0_SCLK
SPI0_SDI
SPI0_SDO
SD1_CLK / GIO24
SD1_CMD / GIO23
SD1_D3 / RTS2 / GIO22
SD1_D2 / CTS2 / GIO21
SD1_D1 / RXD2 / GIO20
SD1_D0 / TXD2 / GIO19
MSSD0_CLK
MSSD0_CMD
MSSD0_DAT3
MSSD0_DAT2
MSSD0_DAT1
MSSD0_DAT0
ASP0_DXRGIO30
ASP0_CLKXGIO29
ASP0_FSXGIO28
ASP0_DRGIO27
ASP0_CLKRGIO26
ASP0_FSRGIO25
ASP1_DX
ASP1_CLKX
ASP1_FSX
ASP1_DR
ASP1_CLKR
ASP1_FSR
ASP1_CLKS
DEEPSLP_EN
ENET_INT
USB_OTG_EN
DM350_TIMERIN
ATA_CE_IO
MSP430_INT
DM350_GIO6
DM350_GIO7

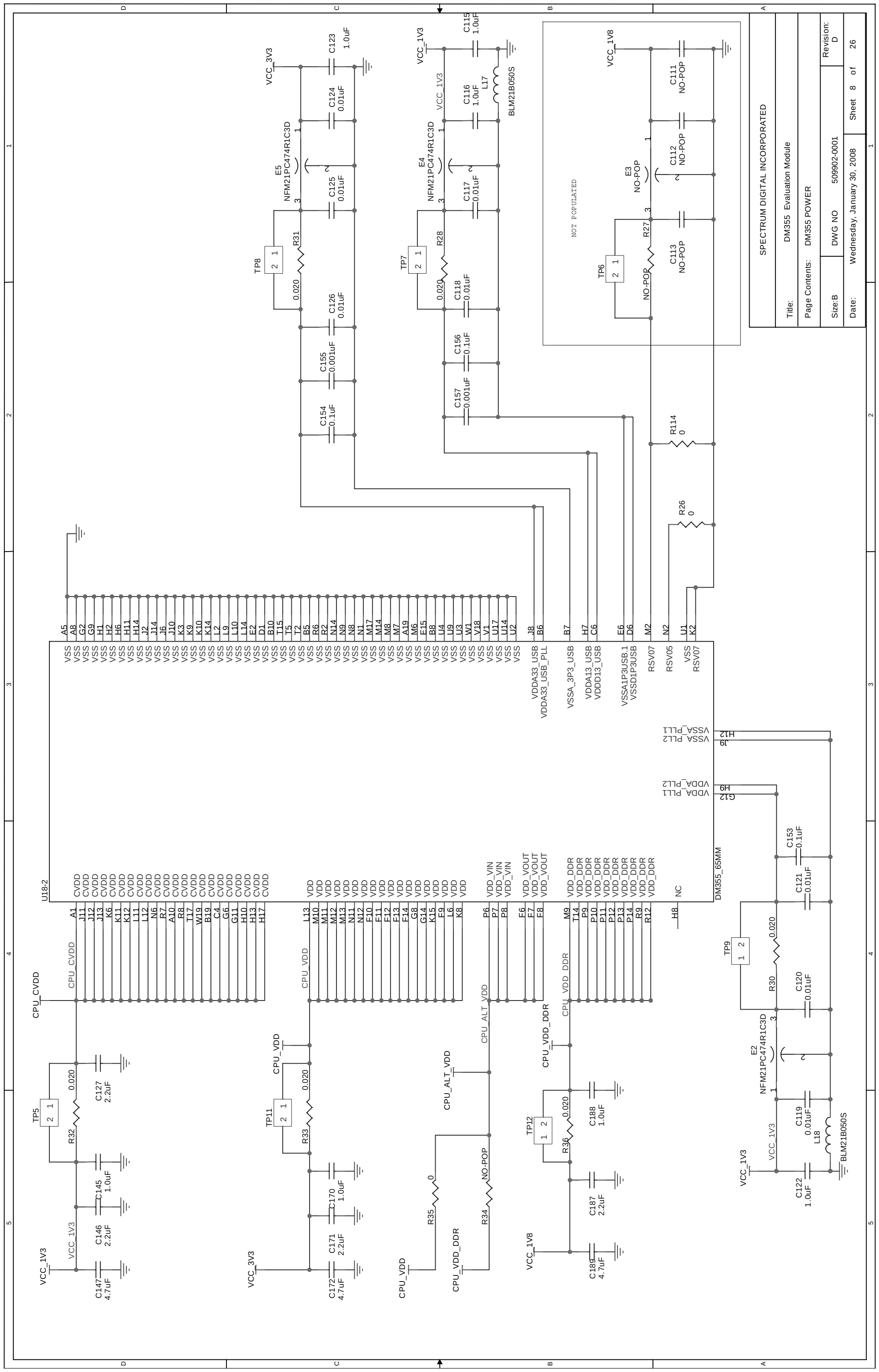

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 DDR INTERFACE
Size:B DWG NO 509902-0001 Revision: D
Date: Friday, March 14, 2008 Sheet 3 of 26
U18:4
DM355_65MM
VCC_3V3
E1
NFM201JP13C105F
C1 2.2uF
C2 0.01uF
C3 0.01uF
R1 0.020
R2 50 OHM 0.5%
R3 0
TP1
VDDA33DDR_DLL
VSSA_DLL
DDR_VREF
DDR_ZN
DDR_CLKP
DDR_CLKN
DDR_CKE
DDR_CS
DDR_WE
DDR_CAS
DDR_RAS
DDR_BA0
DDR_BA1
DDR_BA2
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_A13
DDR_DQ0
DDR_DQ1
DDR_DQ2
DDR_DQ3
DDR_DQ4
DDR_DQ5
DDR_DQ6
DDR_DQ7
DDR_DQ8
DDR_DQ9
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQM0
DDR_DQM1
DDR_DQS0
DDR_DQS1
DDR_GATE0
DDR_GATE1
DDR_STRBEN
DDR_STRBEN_OEL
VREF_STL
Trace to DDR memory
for delay compensation
This net is equal to the DDR_CLKP (or DDR_CLKN)
plus
the length of DDR_DQXX Average Trace length

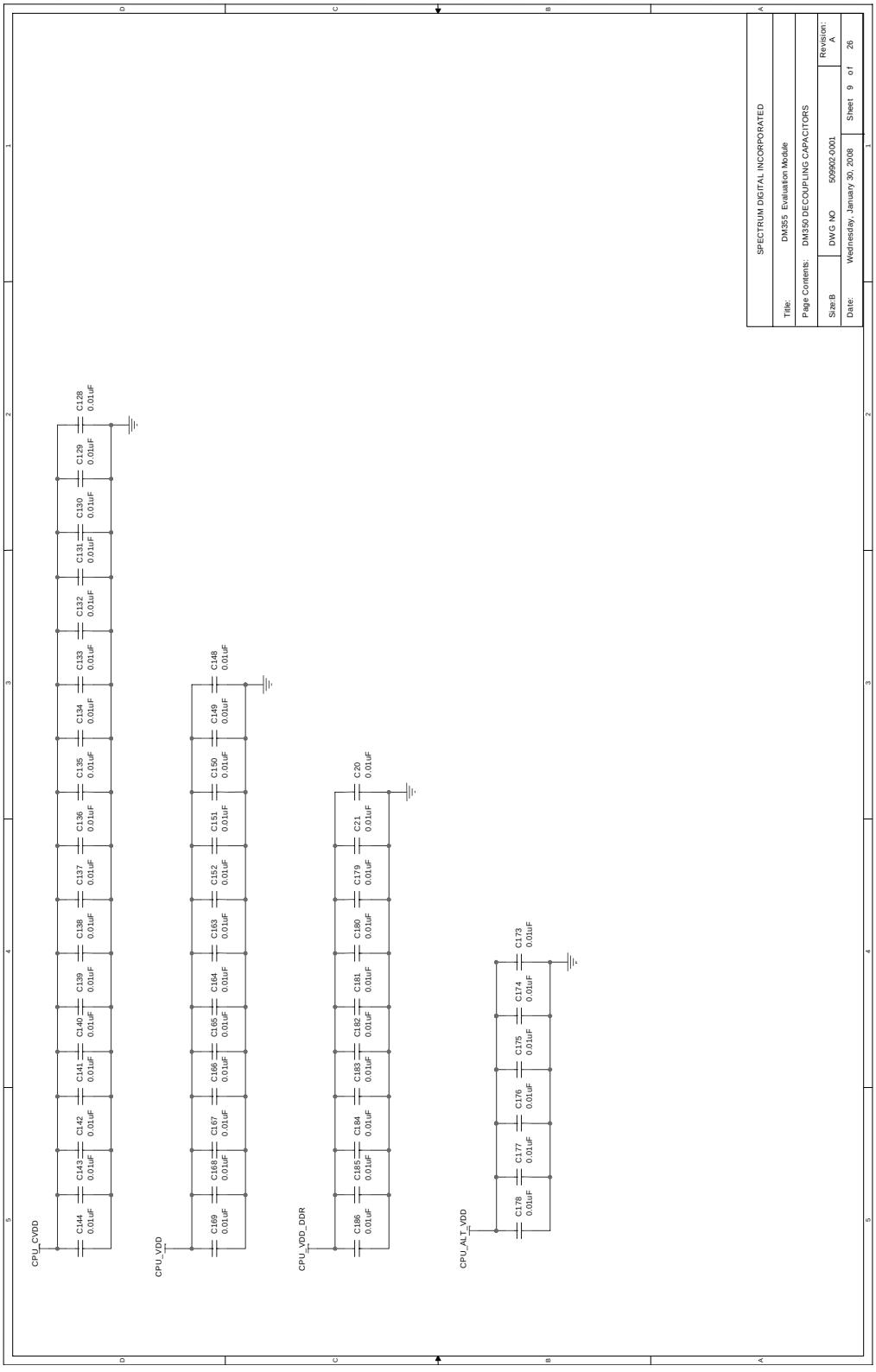

SW7 Boot Select Setting for ARM Boot Mode:
POS 2 | POS 1 | MM CODE
ON | ON | 0 0 | BOOT ROM - NAND LOAD FROM CE0
ON | OFF | 0 1 | NOT AVAILABLE
OFF | ON | 1 0 | BOOT ROM - LOAD FROM SD/MMC
OFF | OFF | 1 1 | BOOT ROM - LOAD FROM UART
Note:
ICE PICK Mode may have an issue booting from Reset
EMU0 = 1, EMU1 = 1
use ARM Mode
EMU0 = 0, EMU1 = 0
See page 11 for more information
SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 EMIF
Size: B | DWG NO 509902-0001 | Revision: C
Date: Friday, March 14, 2008 | Sheet 4 of 26
NAND BOOT STATUS
1 1 0 1 NAND CFG
DM355_65MM
SN74LVC1G08
RPACK4-33

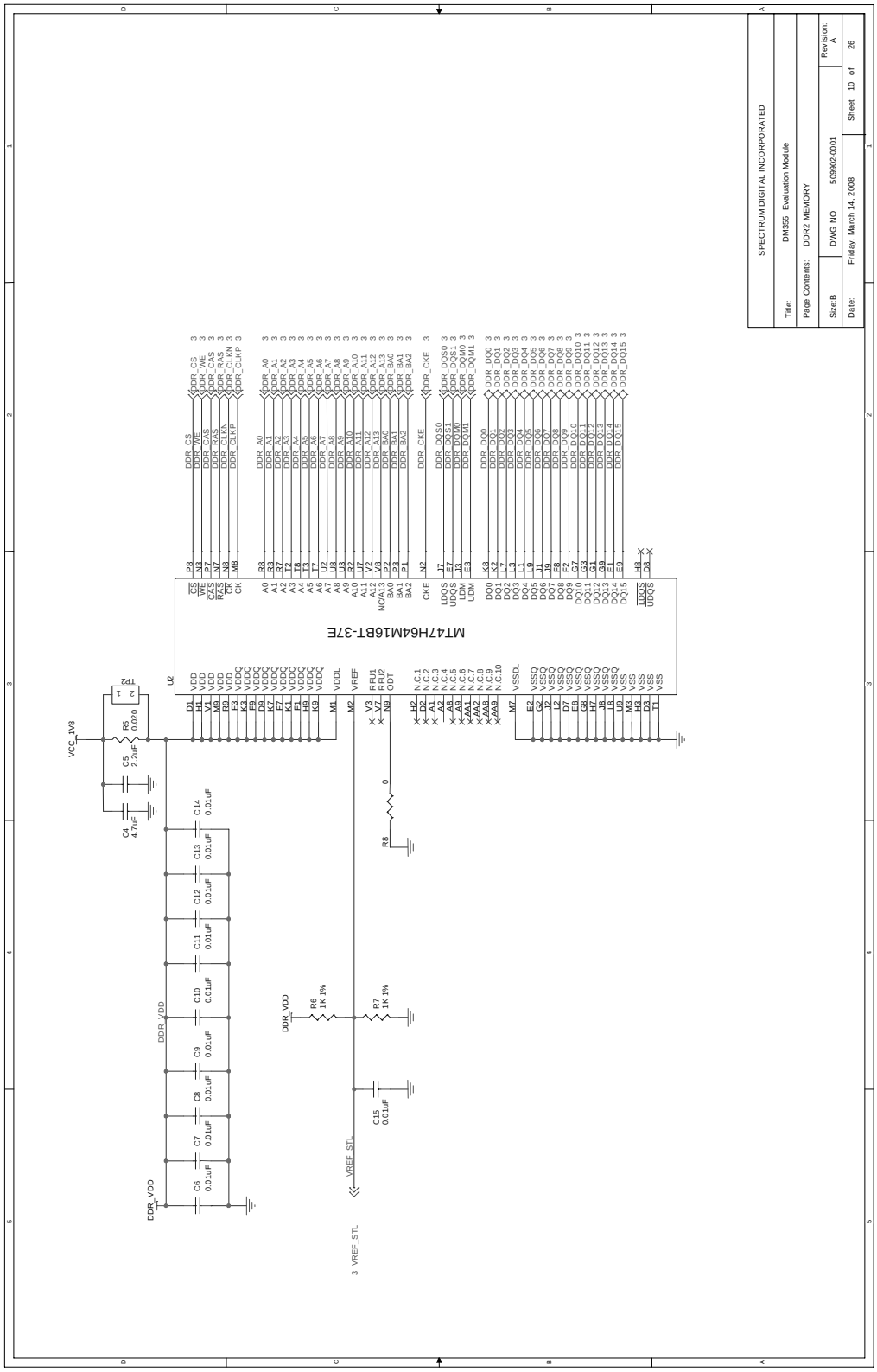

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 USB
Size:B
DWG NO 509902-0001
Revision: D2
Date: Friday, March 14, 2008
Sheet 5 of 26
USE INTERNAL CONTROL REGISTER TO FLIP DM/DP POLARITIES
DIFFERENTIAL PAIR 90 OHM DIFFERENTIAL IMPEDANCE SHORT AND STRAIGHT AS POSSIBLE, MINIMUM NUMBER OF VIAS
NO-POP FOR TEST SPECTRUM DIGITAL TEST ONLY
DIFFERENTIAL PAIRS
PLACE THESE RESISTORS CLOSE TO DM355
SPARE JUMPERS
2 USB_ID_TOGGLE
DM355_65MM
TPS61092RSA
IRLML6401
BSS138
HEADER 2
HEADER 4X2
4 HEADER
BLM21PG221SN1
miniAB

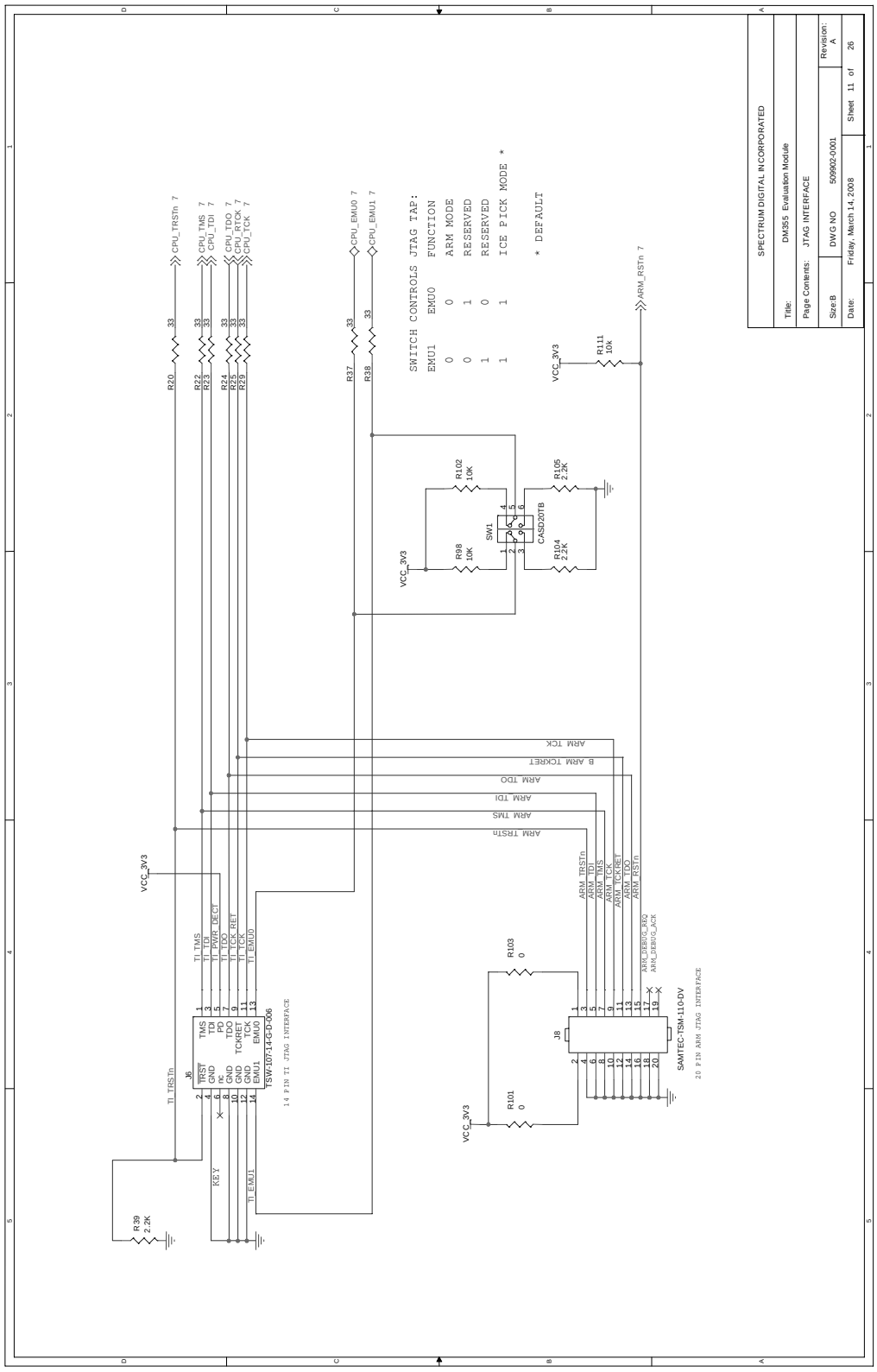

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 VIDEO
Size: B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 6 of 26
U18-6
DM355_ibNM
RPACK4-33
RPACK8-33
RN30
RN31
RN32
J4
RCA JACK
TP13
L19 3uH
L20 BLM21B050S
E6 NFM21PC474R1C3D
R67 1000 1%
R147 1070 1%
R68 2550 1%
R146 0.020
C193 0.1uF
C194 270pF
C195 270pF
C196 2.2uF
C197 0.01uF
C198 0.01uF
VCC_1V8
VDDA_DAC
DSP_GND

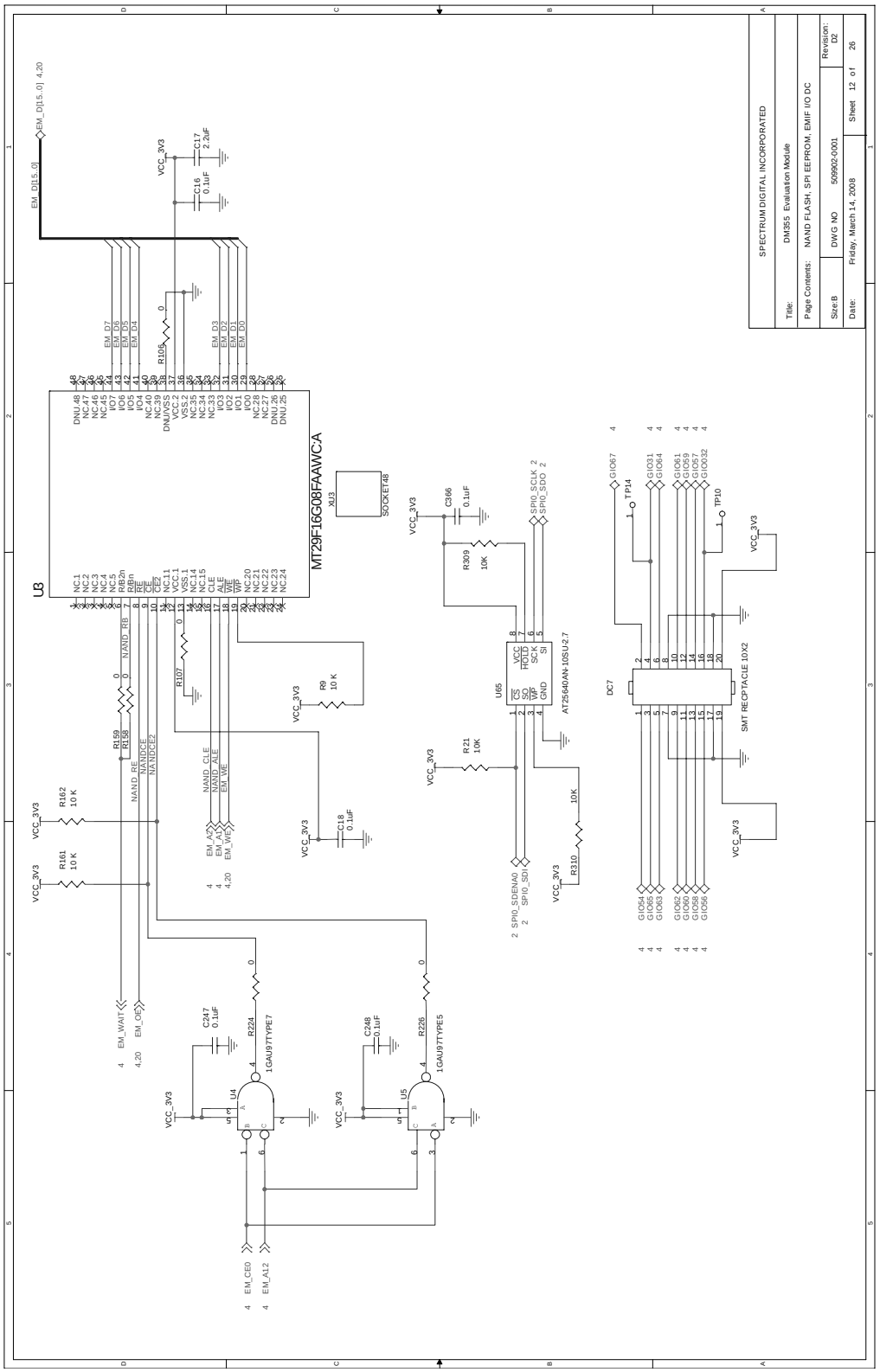

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 JTAG,RESET,CLOCKS
Size:B DWG NO 509902-0001 Revision: A
Date: Friday, March 14, 2008 Sheet 7 of 26
C234 27 pF
C235 27 pF
C236 27 pF
C237 27 pF
TP39
TP40
TP41
TP42
Y3 27MHz
Y2 24MHz
R204 NO-POP
R205 NO-POP
U18-5
MXI2
MXO2
VSS_MX2
MXI1
MXO1
VSS_MX1
GIO18 / CLKOUT1
GIO17 /CLKOUT2
GIO16 / CLKOUT3
DM355_65MM
RESET
TCK
RTCK
TDI
TDO
TMS
TRST
EMU0
EMU1
DM350_RESETn
R347 360
C238 0.1uF
U23
SN74LVC1G08
VCC_3V3
CPU_TCK
CPU_RTCK
CPU_TDI
CPU_TDO
CPU_TMS
CPU_TRSTn
CPU_EMU0
CPU_EMU1
CPU_RESETz
ARM_RSTn

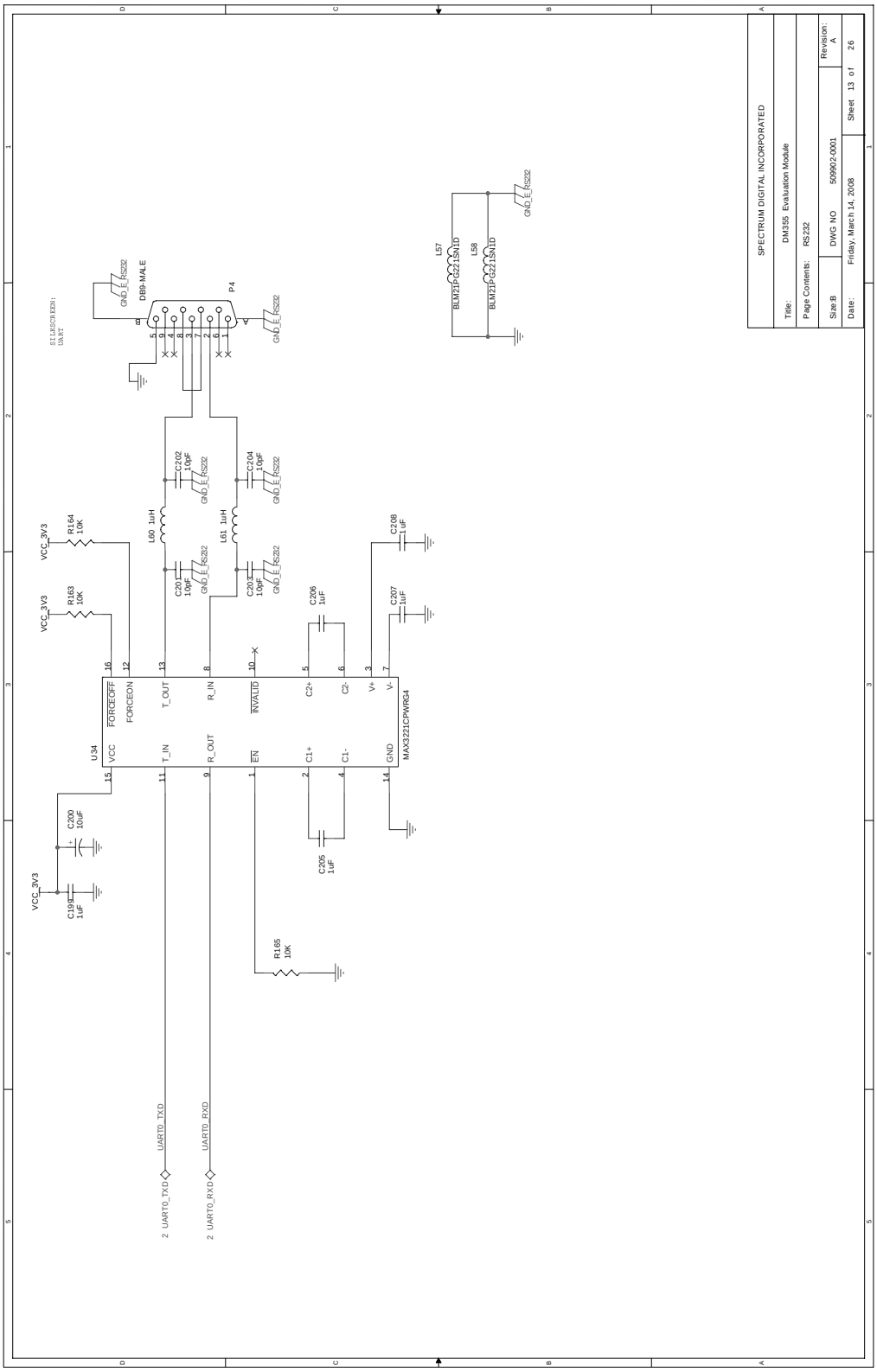

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM355 POWER
Size: B
DWG NO 509902-0001
Revision: D
Date: Wednesday, January 30, 2008
Sheet 8 of 26
NOT POPULATED
U18-2
DM355_65MM

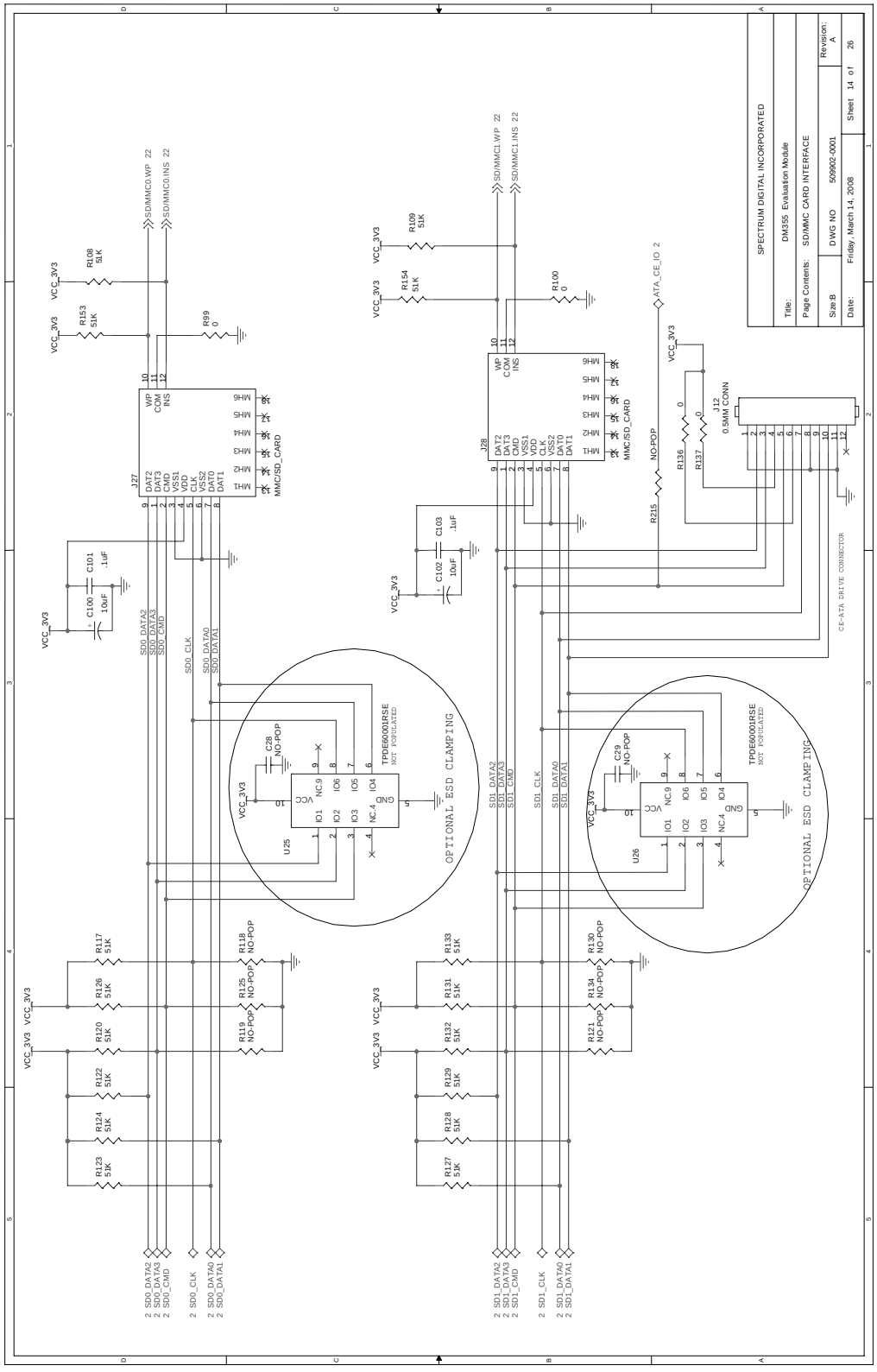

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DM350 DECOUPLING CAPACITORS
Size:B
DWG NO 509902-0001
Revision: A
Date: Wednesday, January 30, 2008
Sheet 9 of 26
CPU_CVDD
CPU_VDD
CPU_VDD_DDR
CPU_ALT_VDD
C144 0.01uF
C143 0.01uF
C142 0.01uF
C141 0.01uF
C140 0.01uF
C139 0.01uF
C138 0.01uF
C137 0.01uF
C136 0.01uF
C135 0.01uF
C134 0.01uF
C133 0.01uF
C132 0.01uF
C131 0.01uF
C130 0.01uF
C129 0.01uF
C128 0.01uF
C169 0.01uF
C168 0.01uF
C167 0.01uF
C166 0.01uF
C165 0.01uF
C164 0.01uF
C163 0.01uF
C152 0.01uF
C151 0.01uF
C150 0.01uF
C149 0.01uF
C148 0.01uF
C196 0.01uF
C185 0.01uF
C184 0.01uF
C183 0.01uF
C182 0.01uF
C181 0.01uF
C180 0.01uF
C179 0.01uF
C21 0.01uF
C20 0.01uF
C178 0.01uF
C177 0.01uF
C176 0.01uF
C175 0.01uF
C174 0.01uF
C173 0.01uF

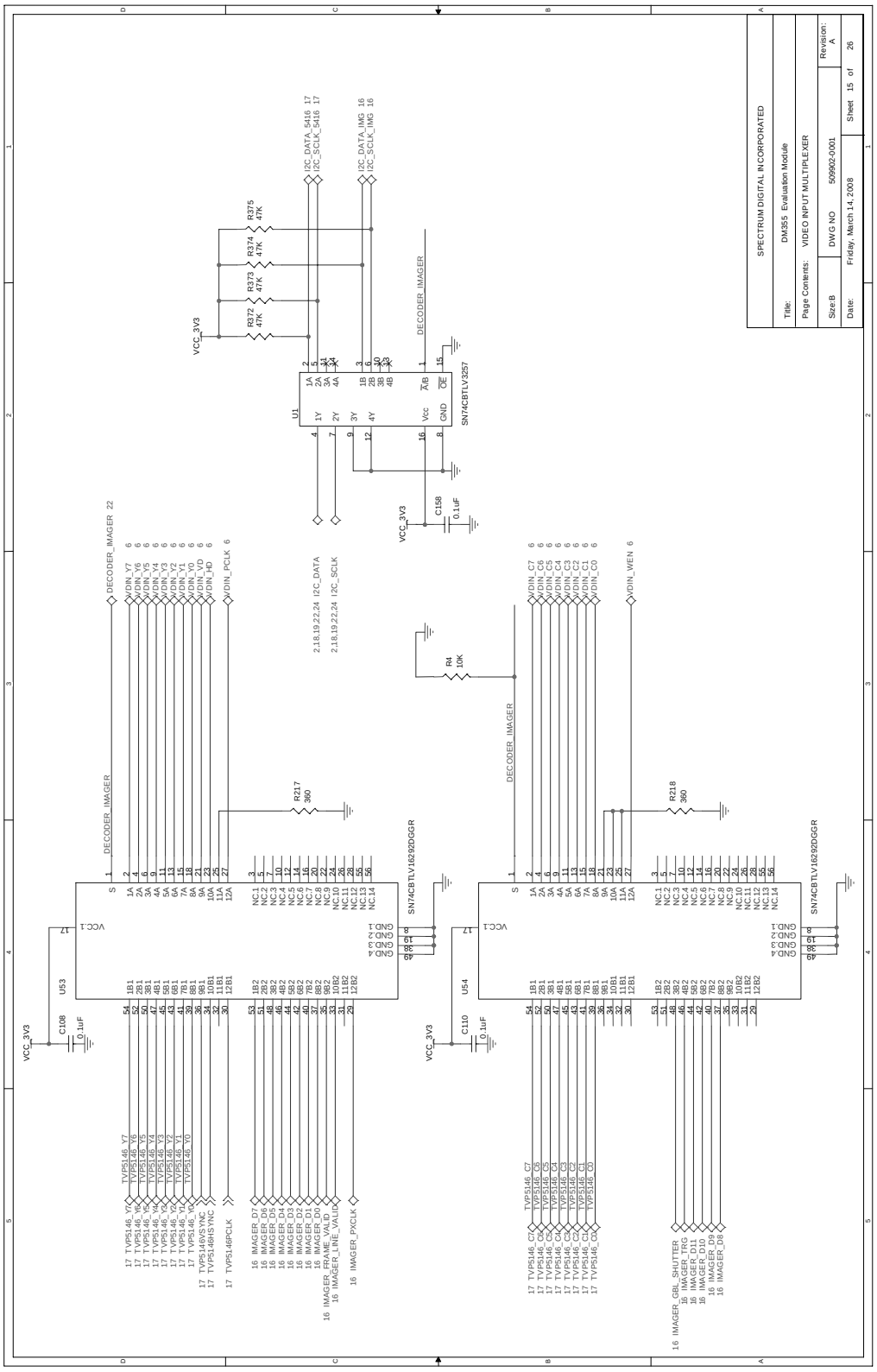

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: DDR2 MEMORY
Size: B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 10 of 26
MT47H64M16BT-37E
U2
VCC_1V8
DDR_VDD
VREF_STL
TP2
R5 0.020
C5 2.2uF
C4 4.7uF
C6 0.01uF
C7 0.01uF
C8 0.01uF
C9 0.01uF
C10 0.01uF
C11 0.01uF
C12 0.01uF
C13 0.01uF
C14 0.01uF
C15 0.01uF
R6 1K 1%
R7 1K 1%
R8 0

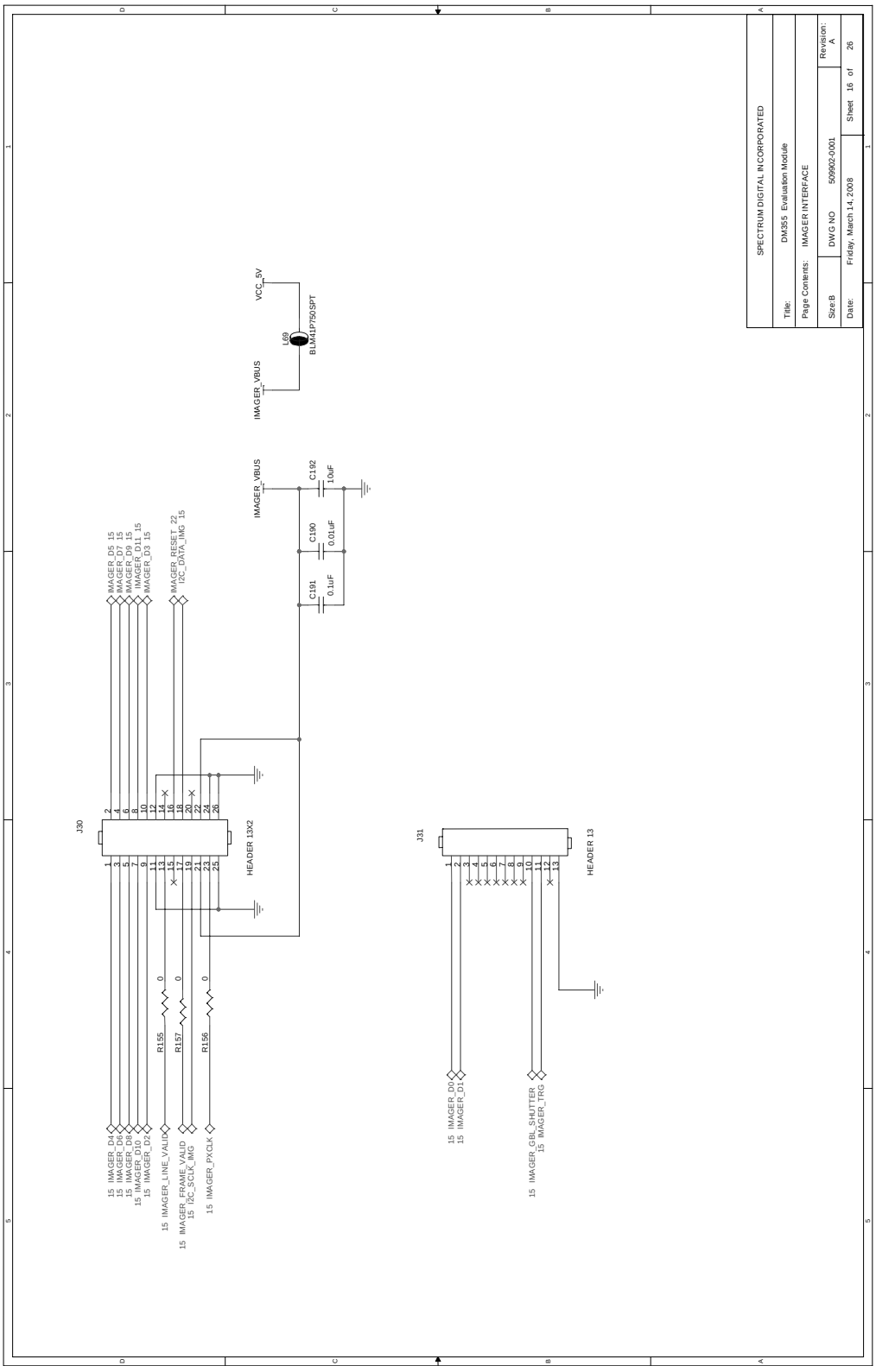

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: JTAG INTERFACE
Size: B
DWG NO 506902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 11 of 26
SWITCH CONTROLS JTAG TAP:
EMU1 EMU0 FUNCTION
0 0 ARM MODE
0 1 RESERVED
1 0 RESERVED
1 1 ICE PICK MODE *
* DEFAULT
J6
TSW-107-14-G-D-006
14 PIN TI JTAG INTERFACE
J8
SAMTEC-TSM-110-DV
20 PIN ARM JTAG INTERFACE
SW1
CAS020TB
R20
R22
R23
R24
R25
R29
R37
R38
R39 2.2K
R98 10K
R102 10K
R104 2.2K
R105 2.2K
R111 10k
R101 0
R103 0
VCC_3V3
CPU_TRSTn 7
CPU_TMS 7
CPU_TDI 7
CPU_TDO 7
CPU_RTCK 7
CPU_TCK 7
CPU_EMU0 7
CPU_EMU1 7
ARM_RSTn 7
TI_TRSTn
TI_TMS
TI_TDI
TI_PWR_DECT
TI_TDO
TI_TCK_RET
TI_TCK
TI_EMU0
TI_EMU1
KEY
ARM TRSTn
ARM TMS
ARM TDI
ARM TDO
B ARM TCKRET
ARM TCK
ARM_TRSTn
ARM_TDI
ARM_TMS
ARM_TCK
ARM_TCKRET
ARM_TDO
ARM_RSTn
ARM_DEBUG_REQ
ARM_DEBUG_ACK

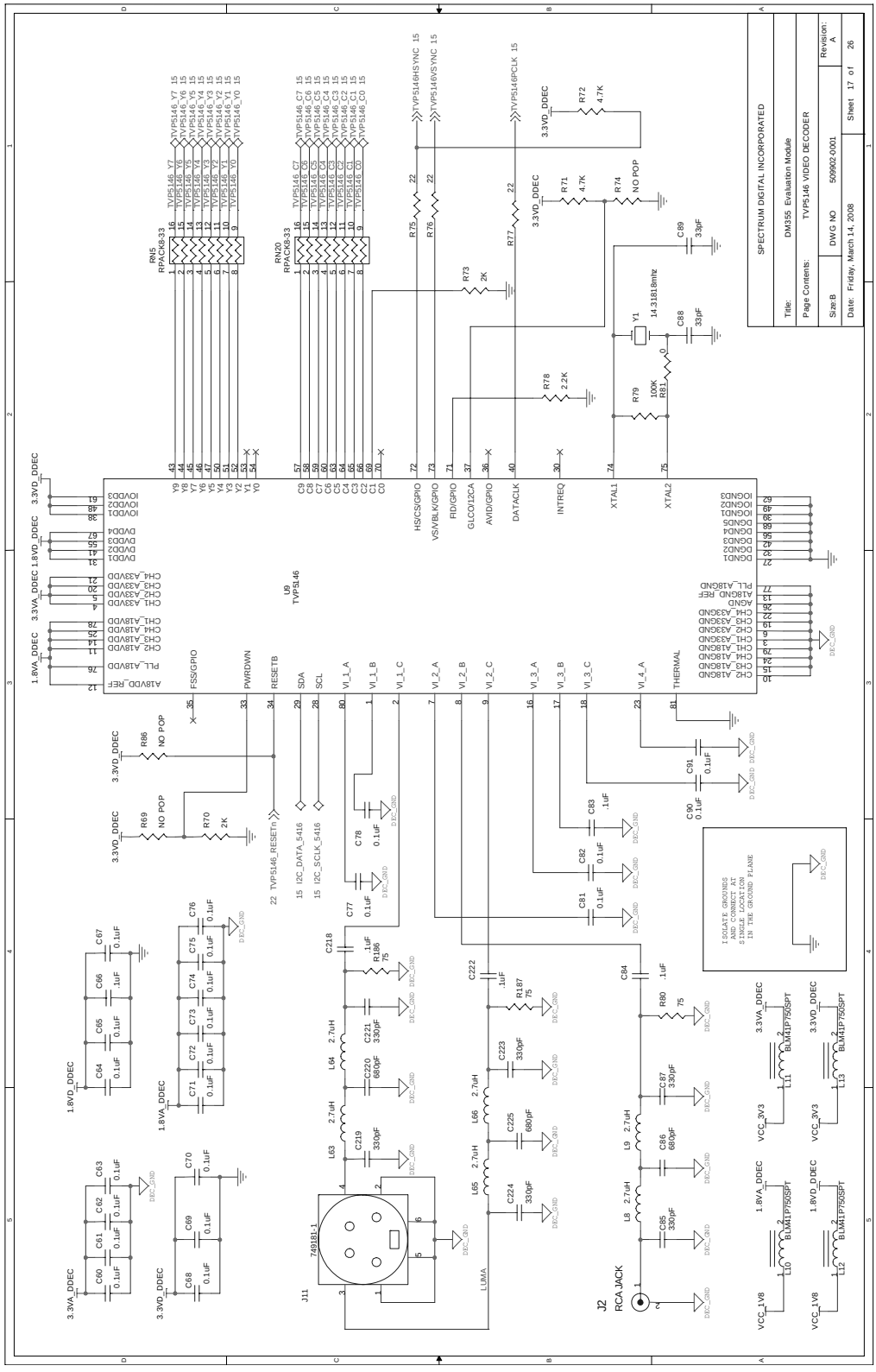

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: NAND FLASH, SPI EEPROM, EMIF I/O DC
Size:B
DWG NO 509902-0001
Revision: D2
Date: Friday, March 14, 2008
Sheet 12 of 26
U8
MT29F16G08FAAWC:A
SOCKET48
U65
AT25640AN-10SU-2.7
DC7
SMT RECPTACLE 10X2
U4
U5
1GAU97TYPE7
1GAU97TYPE5
EM_D[15..0]
VCC_3V3
R159
R158
R162
R161
R107
R9
C18
C247
C248
R224
R226
C16
C17
R105
C366
R309
R21
R310
TP14
TP10
NAND_RB
NANDCE
NANDCE2
NAND_RE
NAND_CLE
NAND_ALE
EM_WE
EM_WAIT
EM_OE
EM_CE0
EM_A12
SPI0_SCLK
SPI0_SDO
SPI0_SDEN
SPI0_SDI
GIO67
GIO31
GIO64
GIO61
GIO59
GIO57
GIO32
GIO54
GIO65
GIO63
GIO62
GIO60
GIO58
GIO56

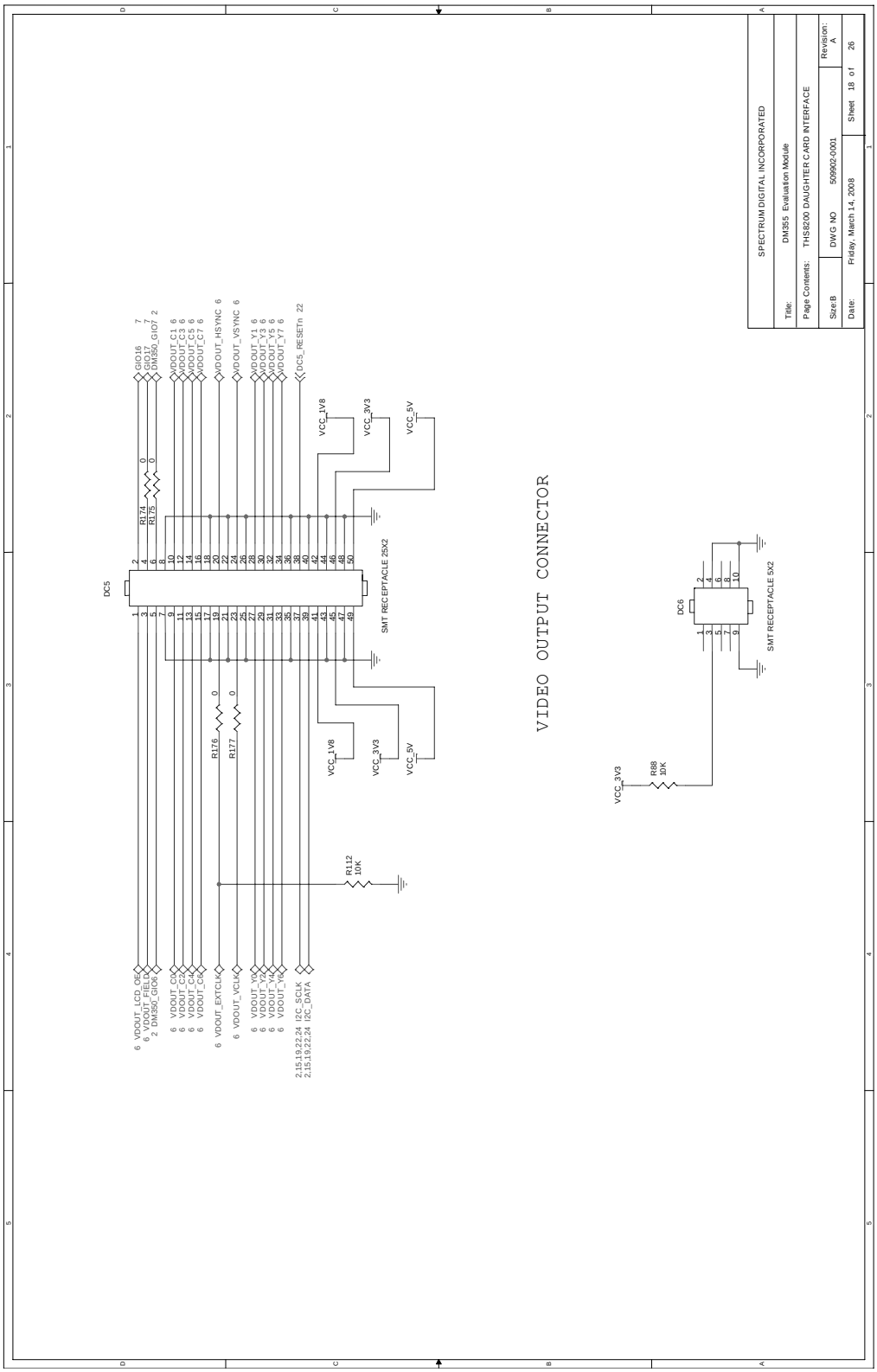

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: RS232
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 13 of 26
U34
MAX3221CPWRG4
VCC
T_IN
R_OUT
EN
C1+
C1-
GND
FORCEOFF
FORCEON
T_OUT
R_IN
INVALID
C2+
C2-
V+
V-
DB9-MALE
P4
L57
L58
BLM21PG221SN1D
L60 1uH
L61 1uH
R164 10K
R163 10K
R165 10K
C200 10uF
C195 10uF
C201 10pF
C202 10pF
C203 10pF
C204 10pF
C205 1uF
C206 1uF
C207 1uF
C208 1uF
VCC_3V3
GND_E_RS232
UART0_TXD
UART0_RXD
2 UART0_TXD
2 UART0_RXD

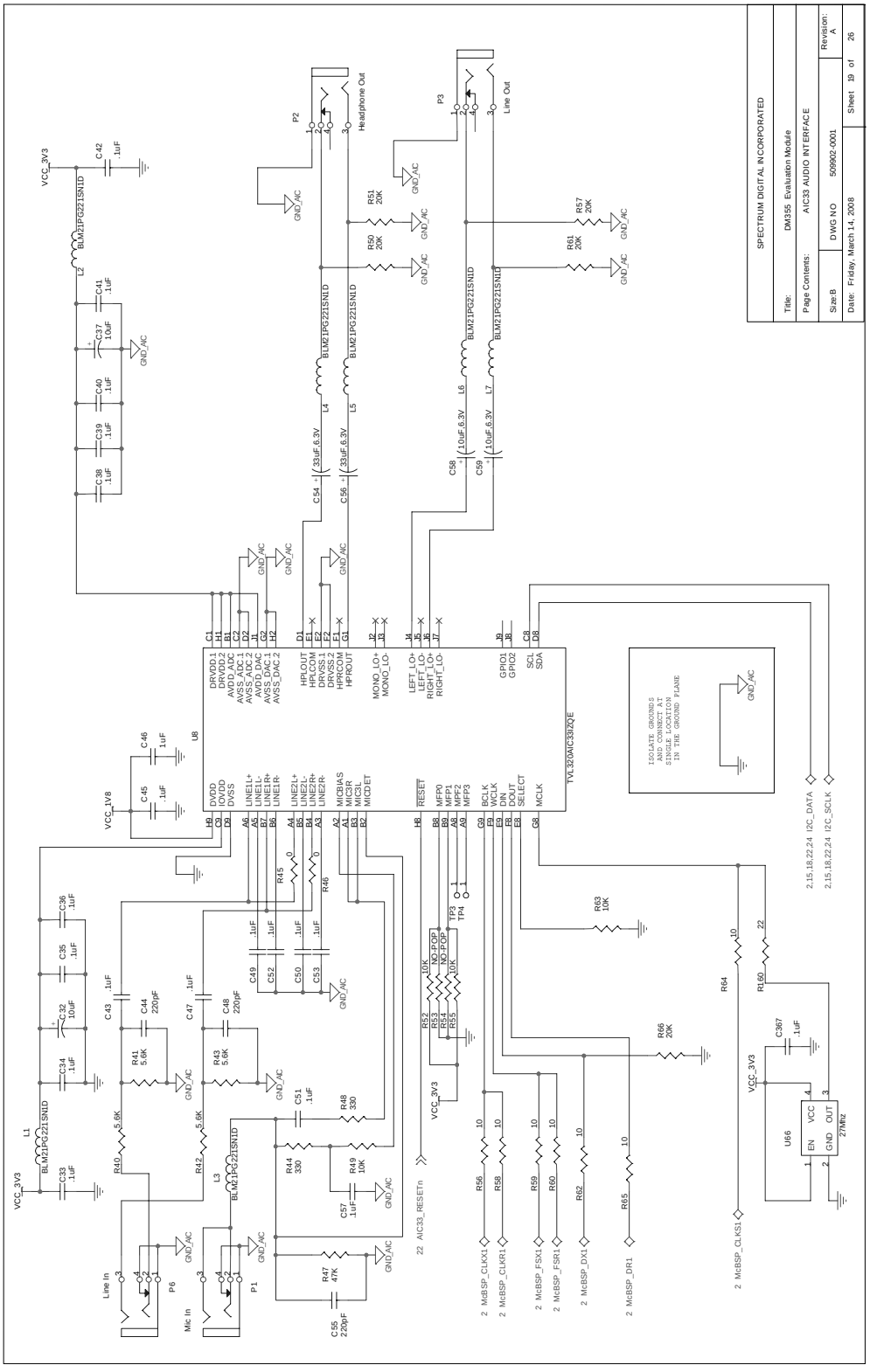

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: SD/MMC CARD INTERFACE
Size:B DWG NO 509902-0001 Revision: A
Date: Friday, March 14, 2008 Sheet 14 of 26
SD/MMC0.WP
SD/MMC0.INS
SD/MMC1.WP
SD/MMC1.INS
MMC/SD_CARD
TPDE6001RSE
NOT POPULATED
OPTIONAL ESD CLAMPING
CE-ATA DRIVE CONNECTOR
0.5MM CONN
ATA_CE_IO 2
SD0_DATA2
SD0_DATA3
SD0_CMD
SD0_CLK
SD0_DATA0
SD0_DATA1
SD1_DATA2
SD1_DATA3
SD1_CMD
SD1_CLK
SD1_DATA0
SD1_DATA1

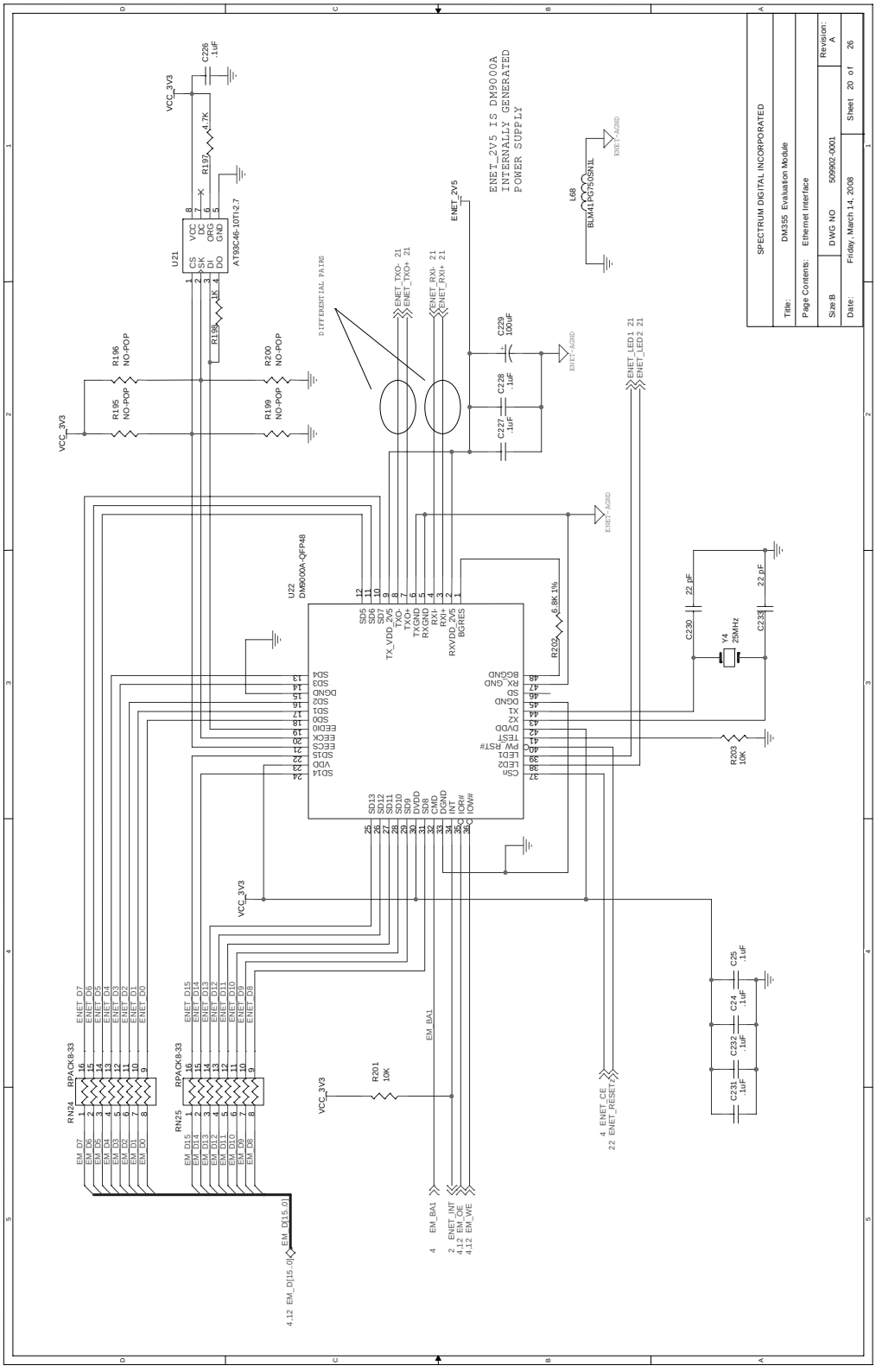

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: VIDEO INPUT MULTIPLEXER
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 15 of 26
U1
SN74CBTLV3257
U53
U54
SN74CBTLV16292DGGR
DECODER_IMAGER
VCC_3V3
C108 0.1uF
C110 0.1uF
C158 0.1uF
R4 10K
R217 360
R218 360
R372 47K
R373 47K
R374 47K
R375 47K
I2C_DATA_5416
I2C_SCLK_5416
I2C_DATA_IMG
I2C_SCLK_IMG
I2C_DATA
I2C_SCLK
TVP5146_Y7
TVP5146_Y6
TVP5146_Y5
TVP5146_Y4
TVP5146_Y3
TVP5146_Y2
TVP5146_Y1
TVP5146_Y0
TVP5146_C7
TVP5146_C6
TVP5146_C5
TVP5146_C4
TVP5146_C3
TVP5146_C2
TVP5146_C1
TVP5146_C0
TVP5146_VSYNC
TVP5146_HSYNC
TVP5146_PCLK
IMAGER_D7
IMAGER_D6
IMAGER_D5
IMAGER_D4
IMAGER_D3
IMAGER_D2
IMAGER_D1
IMAGER_D0
IMAGER_FRAME_VALID
IMAGER_LINE_VALID
IMAGER_PXCLK
IMAGER_GBL_SHUTTER
IMAGER_TRG
IMAGER_D11
IMAGER_D10
IMAGER_D9
IMAGER_D8
VDIN_Y7
VDIN_Y6
VDIN_Y5
VDIN_Y4
VDIN_Y3
VDIN_Y2
VDIN_Y1
VDIN_Y0
VDIN_VD
VDIN_HD
VDIN_PCLK
VDIN_C7
VDIN_C6
VDIN_C5
VDIN_C4
VDIN_C3
VDIN_C2
VDIN_C1
VDIN_C0
VDIN_WEN

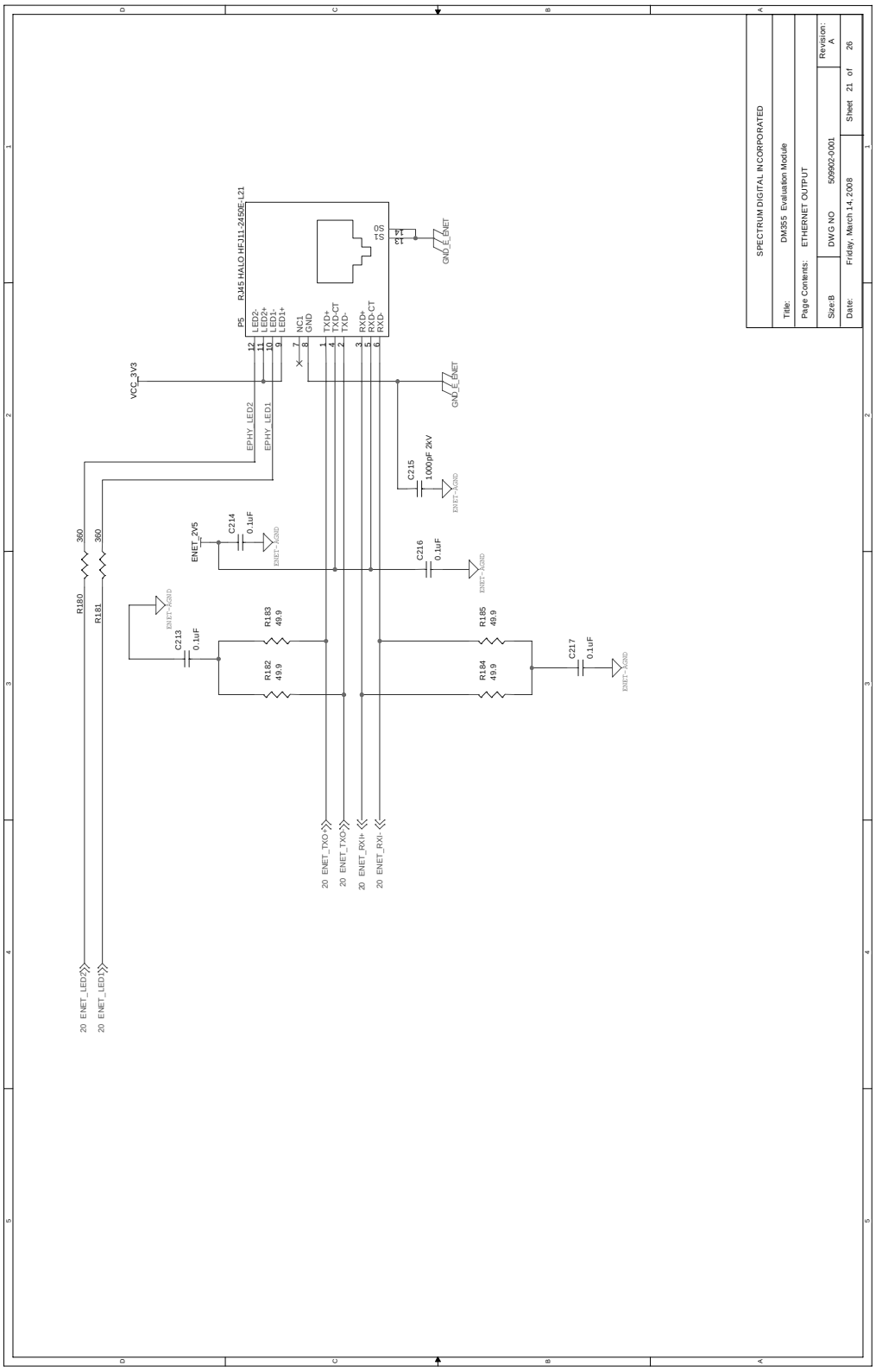

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: IMAGER INTERFACE
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 16 of 26
VCC_5V
L69
BLM41P750SPT
IMAGER_VBUS
C192
10uF
C190
0.01uF
C191
0.1uF
J30
HEADER 13X2
J31
HEADER 13
R155
R157
R156
IMAGER_D5 15
IMAGER_D7 15
IMAGER_D9 15
IMAGER_D11 15
IMAGER_D13 15
IMAGER_RESET 22
I2C_DATA_IMG 15
15 IMAGER_D4
15 IMAGER_D6
15 IMAGER_D8
15 IMAGER_D10
15 IMAGER_D12
15 IMAGER_LINE_VALID
15 IMAGER_FRAME_VALID
15 I2C_SCLK_IMG
15 IMAGER_PXCLK
15 IMAGER_D0
15 IMAGER_D1
15 IMAGER_GBL_SHUTTER
15 IMAGER_TRG

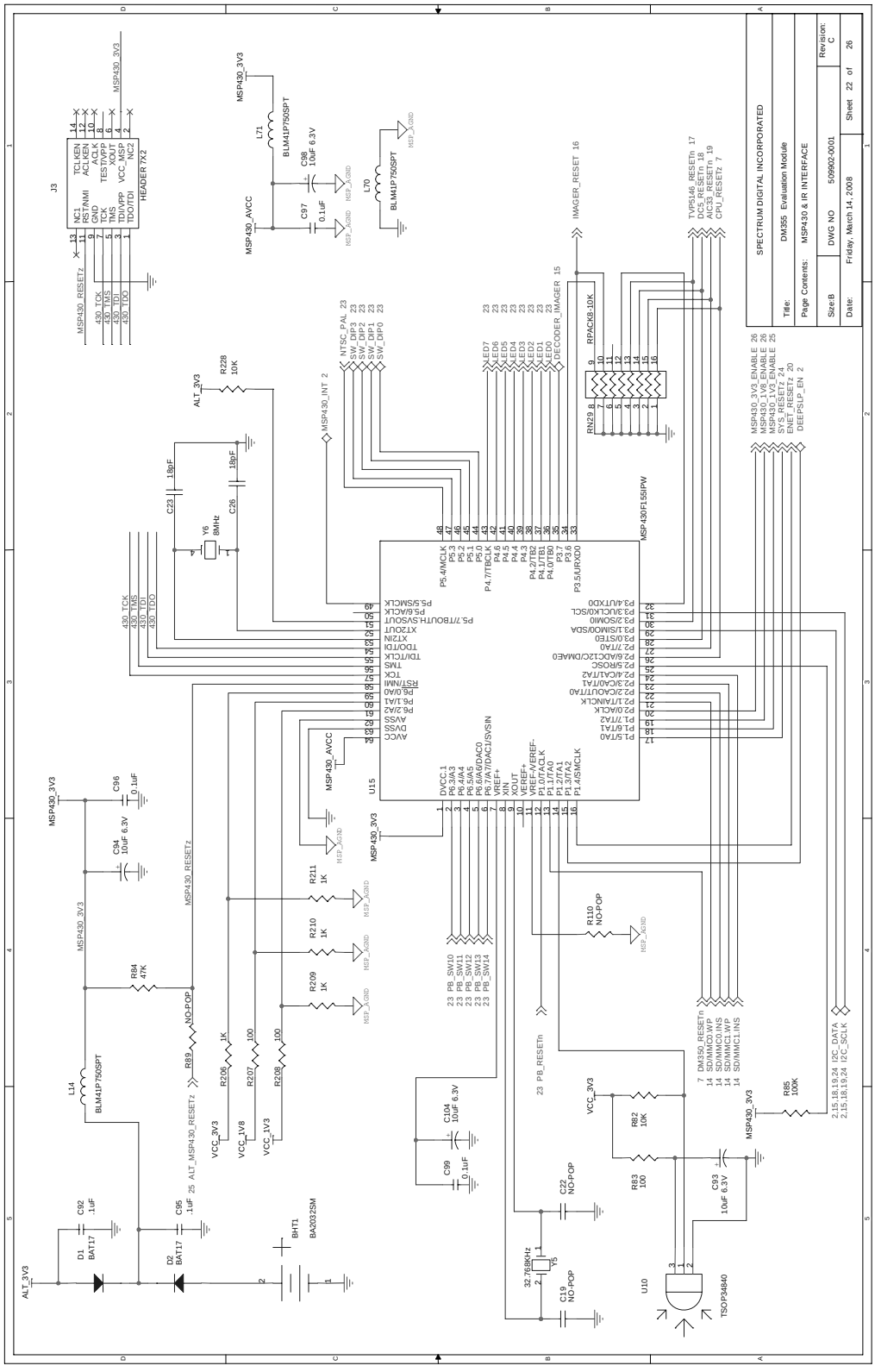

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: TVP5146 VIDEO DECODER
Size: B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 17 of 26
U9
TVP5146
RN5
RPACK8-33
RN20
RPACK8-33
Y1
14.31818mhz
J2
RCA JACK
J11
74918T-1
LUMA
ISOLATE GROUNDS
AND CONNECT AT A
SINGLE LOCATION
IN THE GROUND PLANE
I2C_DATA_5416
I2C_SCLK_5416
TVP5146_RESET(n)

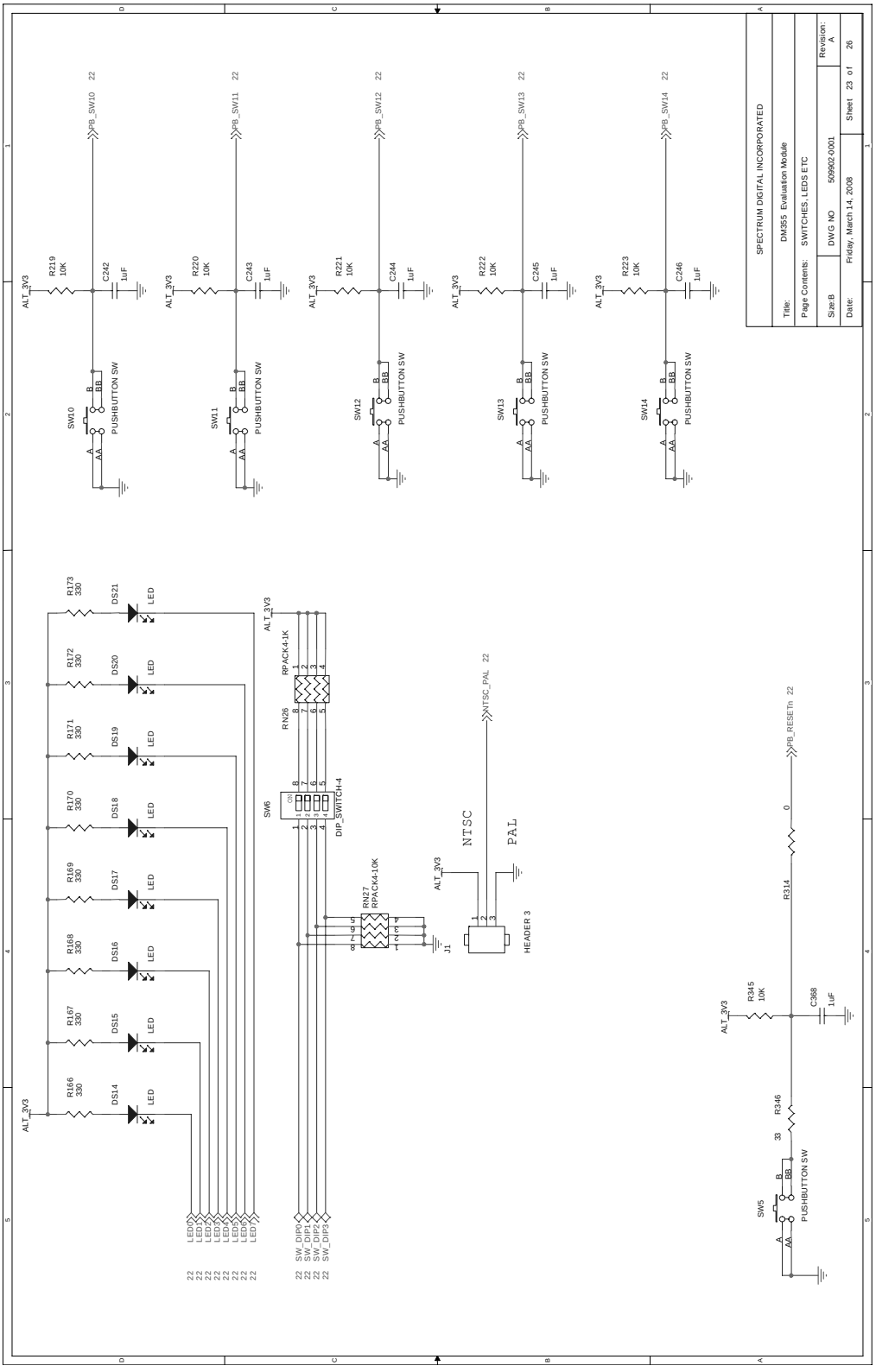

VIDEO OUTPUT CONNECTOR
SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: THS8200 DAUGHTER CARD INTERFACE
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 18 of 26
DC5
SMT RECEPTACLE 25X2
DC6
SMT RECEPTACLE 5X2
R174 0
R175 0
R176 0
R177 0
R112 10K
R88 10K
VCC_1V8
VCC_3V3
VCC_5V
GIO16
GIO17
DM350_GIO7
VDOUT_C1
VDOUT_C3
VDOUT_C5
VDOUT_C7
VDOUT_HSYNC
VDOUT_VSYNC
VDOUT_Y1
VDOUT_Y3
VDOUT_Y5
VDOUT_Y7
DC5_RESETn
VDOUT_LCD_OE
VDOUT_FIELD
DM350_GIO6
VDOUT_C0
VDOUT_C2
VDOUT_C4
VDOUT_C6
VDOUT_EXTCLK
VDOUT_VCLK
VDOUT_Y0
VDOUT_Y2
VDOUT_Y4
VDOUT_Y6
I2C_SCLK
I2C_DATA

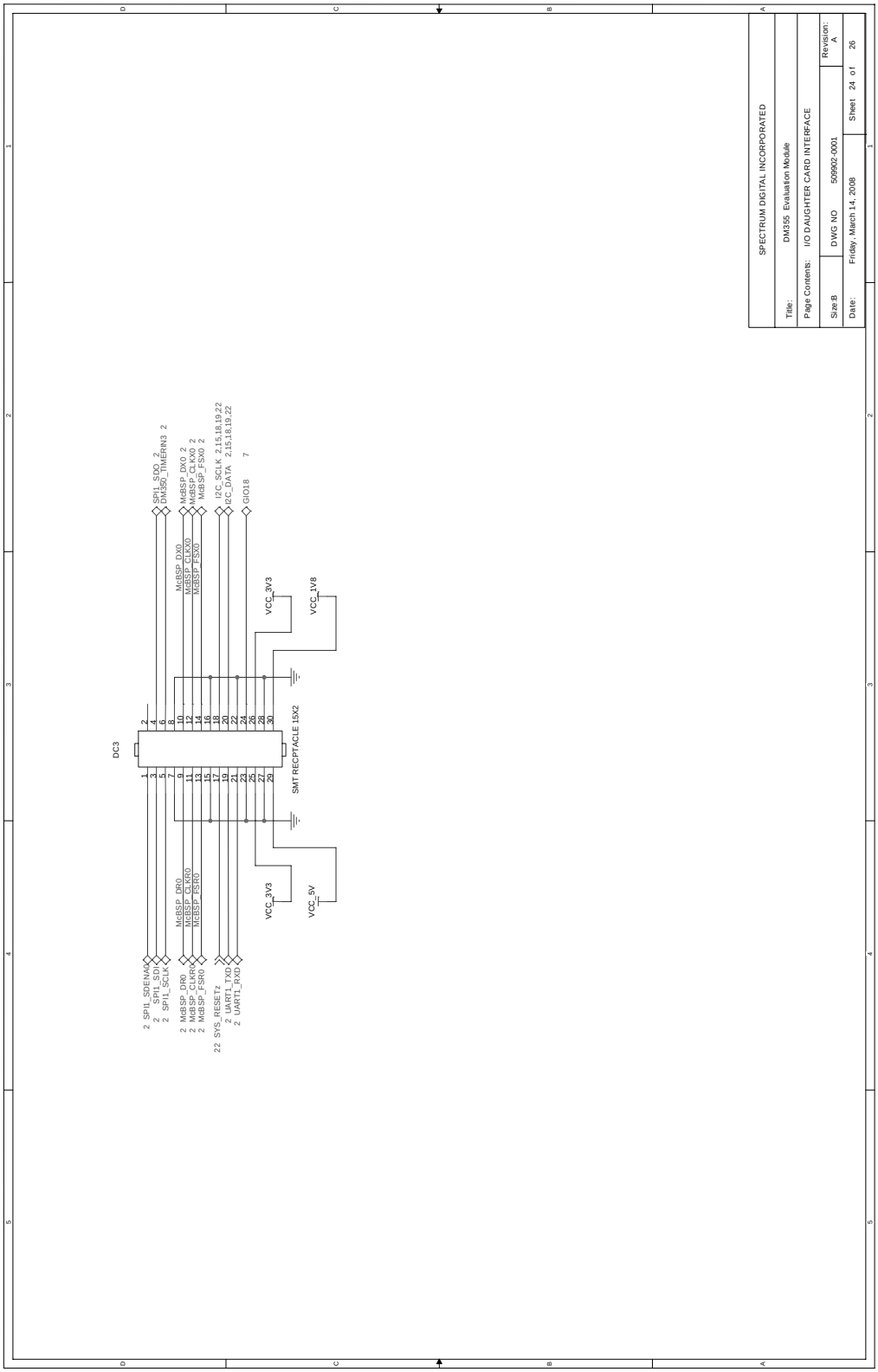

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: AIC33 AUDIO INTERFACE
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 19 of 26
TVL320AIC33IZQE
Headphone Out
Line Out
Line In
Mic In
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE
2.15,18,22,24 I2C_DATA
2.15,18,22,24 I2C_SCLK
22 AIC33_RESETn
2 McBSP_CLKX1
2 McBSP_CLKR1
2 McBSP_FSX1
2 McBSP_FSR1
2 McBSP_DX1
2 McBSP_DR1
2 McBSP_CLKS1
27Mhz

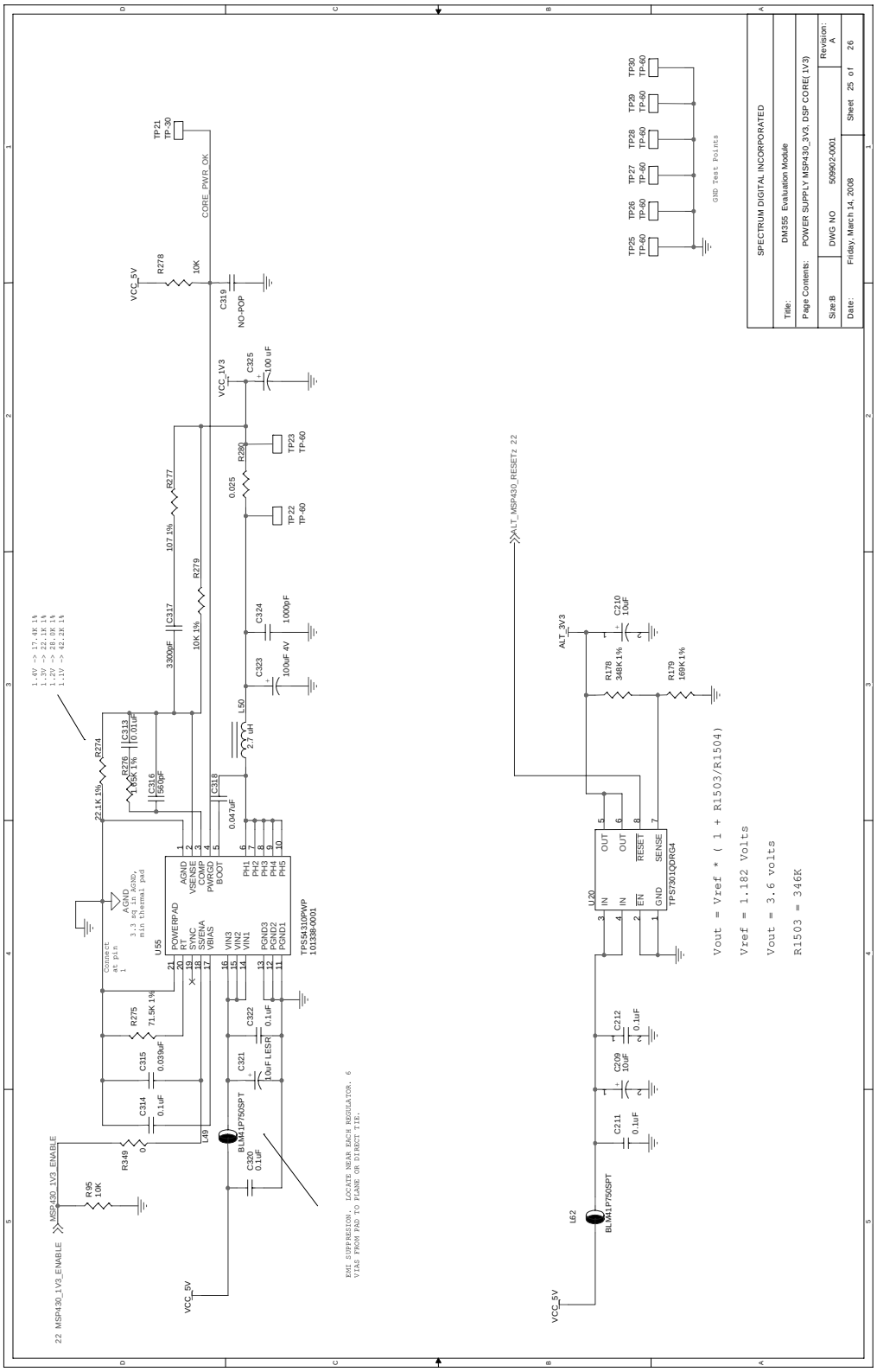

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: Ethernet Interface
Size:B DWG NO 509902-0001 Revision: A
Date: Friday, March 14, 2008 Sheet 20 of 26
ENET_2V5 IS DM9000A INTERNALLY GENERATED POWER SUPPLY
DIFFERENTIAL PAIRS
U21 AT93C46-10TI-2.7
U22 DM9000A-QFP48
VCC_3V3
ENET_2V5
ENET-AGND
R196 NO-POP
R195 NO-POP
R200 NO-POP
R199 NO-POP
R188 1K
R197 4.7K
C226 .1uF
C229 100uF
C228 .1uF
C227 .1uF
L68 BLM41PG750SN1L
R202 6.8K 1%
C230 22 pF
C233 22 pF
Y4 25MHz
R203 10K
R201 10K
RN24 RPACK8-33
RN25 RPACK8-33
C231 .1uF
C232 .1uF
C24 .1uF
C25 .1uF
ENET_LED1 21
ENET_LED2 21
ENET_TXO- 21
ENET_TXO+ 21
ENET_RXI- 21
ENET_RXI+ 21
4 ENET_CE
22 ENET_RESET
4 EM_BA1
2 ENET_INT
4,12 EM_OE
4,12 EM_WE
4,12 EM_D[15..0]

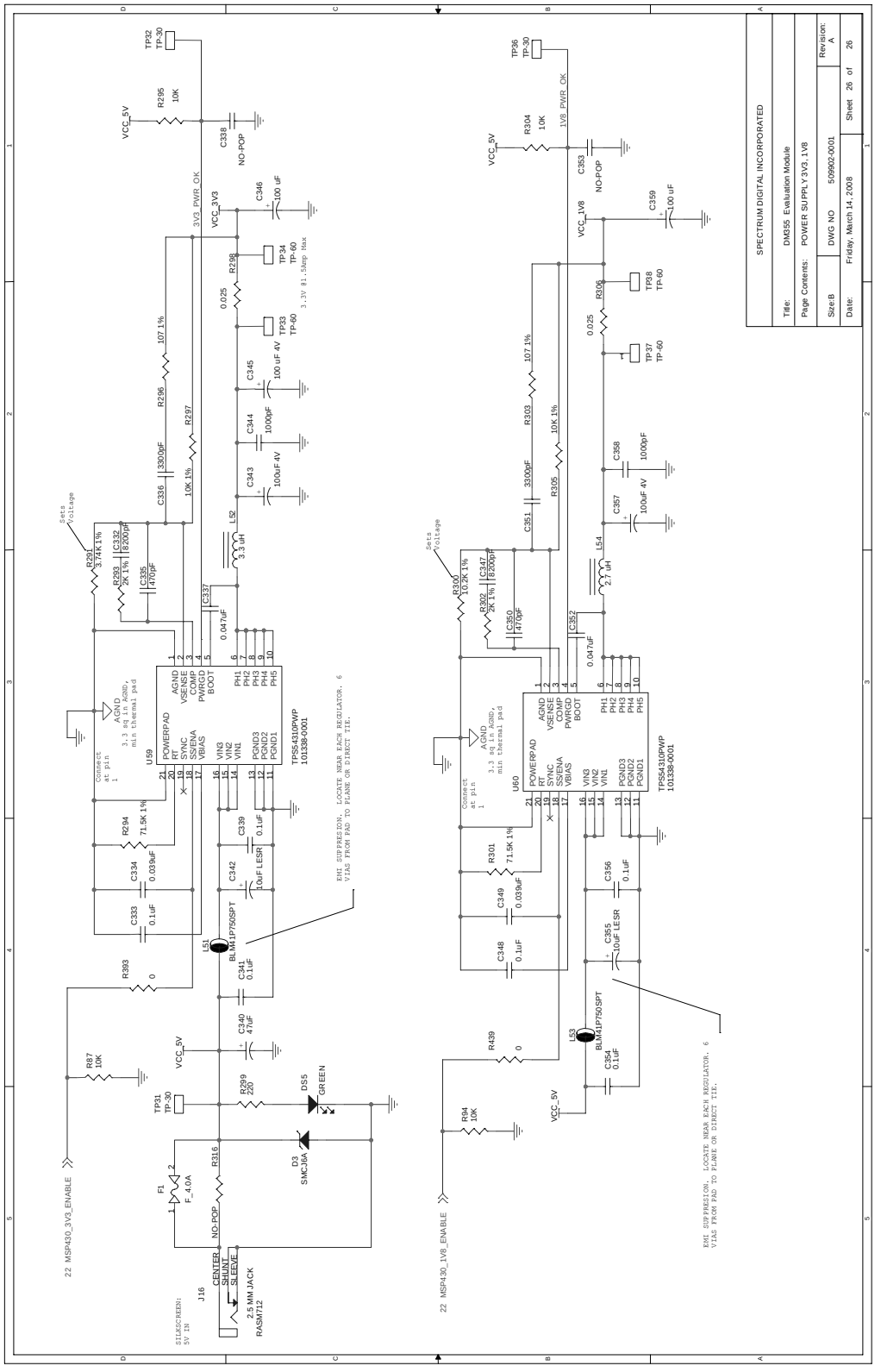

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: ETHERNET OUTPUT
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 21 of 26
P5 RJ45 HALO HFJ11-2450E-L21
LED2-
LED2+
LED1-
LED1+
NC1
GND
TXD+
TXD-CT
TXD-
RXD+
RXD-CT
RXD-
VCC_3V3
GND_E_ENET
EPHY_LED2
EPHY_LED1
C215 1000pF 2kV
C214 0.1uF
C216 0.1uF
C213 0.1uF
C217 0.1uF
ENET_2V5
ENET_AGND
R180 360
R181 360
R183 49.9
R182 49.9
R185 49.9
R184 49.9
20 ENET_LED2
20 ENET_LED1
20 ENET_TXO+
20 ENET_TXO-
20 ENET_RXI+
20 ENET_RXI-


SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: MSP430 & IR INTERFACE
Size: B
DWG NO 509902-0001
Revision: C
Date: Friday, March 14, 2008
Sheet 22 of 26
J3
HEADER 7X2
U15
MSP430F155IPW
U10
TSOP34840
BH1
BA2032SM
L14
BLM41P750SPT
L71
BLM41P750SPT
L70
BLM41P750SPT
Y6
8MHz
Y5
32.768KHz
D1
BAT17
D2
BAT17
RPACK8-10K
RN29.8
MSP430_3V3
ALT_3V3
VCC_3V3
VCC_1V8
VCC_1V3
MSP430_AVCC
MSP430_RESETz
ALT_MSP430_RESETz
MSP430_INT 2
NTSC_PAL 23
SW_DIP3 23
SW_DIP2 23
SW_DIP1 23
SW_DIP0 23
LED7 23
LED6 23
LED5 23
LED4 23
LED3 23
LED2 23
LED1 23
LED0 23
DECODER_IMAGER 15
IMAGER_RESET 16
TVP5146_RESETn 17
DC5_RESETn 18
AIC23_RESETn 19
CPU_RESETz 7
MSP430_3V3_ENABLE 26
MSP430_1V8_ENABLE 25
MSP430_1V3_ENABLE 25
SYS_RESETz 24
ENET_RESETz 20
DEEPSLP_EN 2
PB_RESETn 23
PB_SW10 23
PB_SW11 23
PB_SW12 23
PB_SW13 23
PB_SW14 23
DM350_RESETn 7
SD/MMC0.WP 14
SD/MMC0.INS 14
SD/MMC1.WP 14
SD/MMC1.INS 14
I2C_DATA 2,15,18,19,24
I2C_SCLK 2,15,18,19,24
C23 18pF
C26 18pF
C92 .1uF
C95 .1uF
C96 0.1uF
C94 10uF 6.3V
C97 0.1uF
C98 10uF 6.3V
C104 10uF 6.3V
C99 0.1uF
C93 10uF 6.3V
C22 NO-POP
C19 NO-POP
R228 10K
R84 47K
R89 NO-POP
R206 1K
R207 100
R208 100
R209 1K
R210 1K
R211 1K
R110 NO-POP
R82 10K
R83 100
R85 100K


SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: SWITCHES, LED'S ETC
Size:B DWG NO 509902-0001 Revision: A
Date: Friday, March 14, 2008 Sheet 23 of 26
PB_SW10
PB_SW11
PB_SW12
PB_SW13
PB_SW14
PB_RESETn
NTSC_PAL
ALT_3V3
R219 10K
R220 10K
R221 10K
R222 10K
R223 10K
C242 1uF
C243 1uF
C244 1uF
C245 1uF
C246 1uF
SW10 PUSHBUTTON SW
SW11 PUSHBUTTON SW
SW12 PUSHBUTTON SW
SW13 PUSHBUTTON SW
SW14 PUSHBUTTON SW
R173 330
R172 330
R171 330
R170 330
R169 330
R168 330
R167 330
R166 330
DS21 LED
DS20 LED
DS19 LED
DS18 LED
DS17 LED
DS16 LED
DS15 LED
DS14 LED
LED7
LED6
LED5
LED4
LED3
LED2
LED1
LED0
SW6 DIP_SWITCH-4
SW_DIP0
SW_DIP1
SW_DIP2
SW_DIP3
RN26 RPACK4-1K
RN27 RPACK4-10K
J1 HEADER 3
NTSC
PAL
R314 0
R345 10K
C368 1uF
R346 33
SW5 PUSHBUTTON SW


SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: I/O DAUGHTER CARD INTERFACE
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 24 of 26
DC3
SMT RECPTACLE 15X2
SPI1_SDO_2
DM350_TIMERIN3 2
McBSP_DX0_2
McBSP_CLKX0 2
McBSP_FSX0 2
I2C_SCLK 2,15,18,19,22
I2C_DATA 2,15,18,19,22
GIO18 7
McBSP_DX0
McBSP_CLKX0
McBSP_FSX0
VCC_3V3
VCC_1V8
VCC_3V3
VCC_5V
2 SPI1_SDENA0
2 SPI1_SDI
2 SPI1_SCLK
2 McBSP_DR0
2 McBSP_CLKR0
2 McBSP_FSR0
22 SYS_RESET2
2 UART1_TXD
2 UART1_RXD
McBSP_DR0
McBSP_CLKR0
McBSP_FSR0

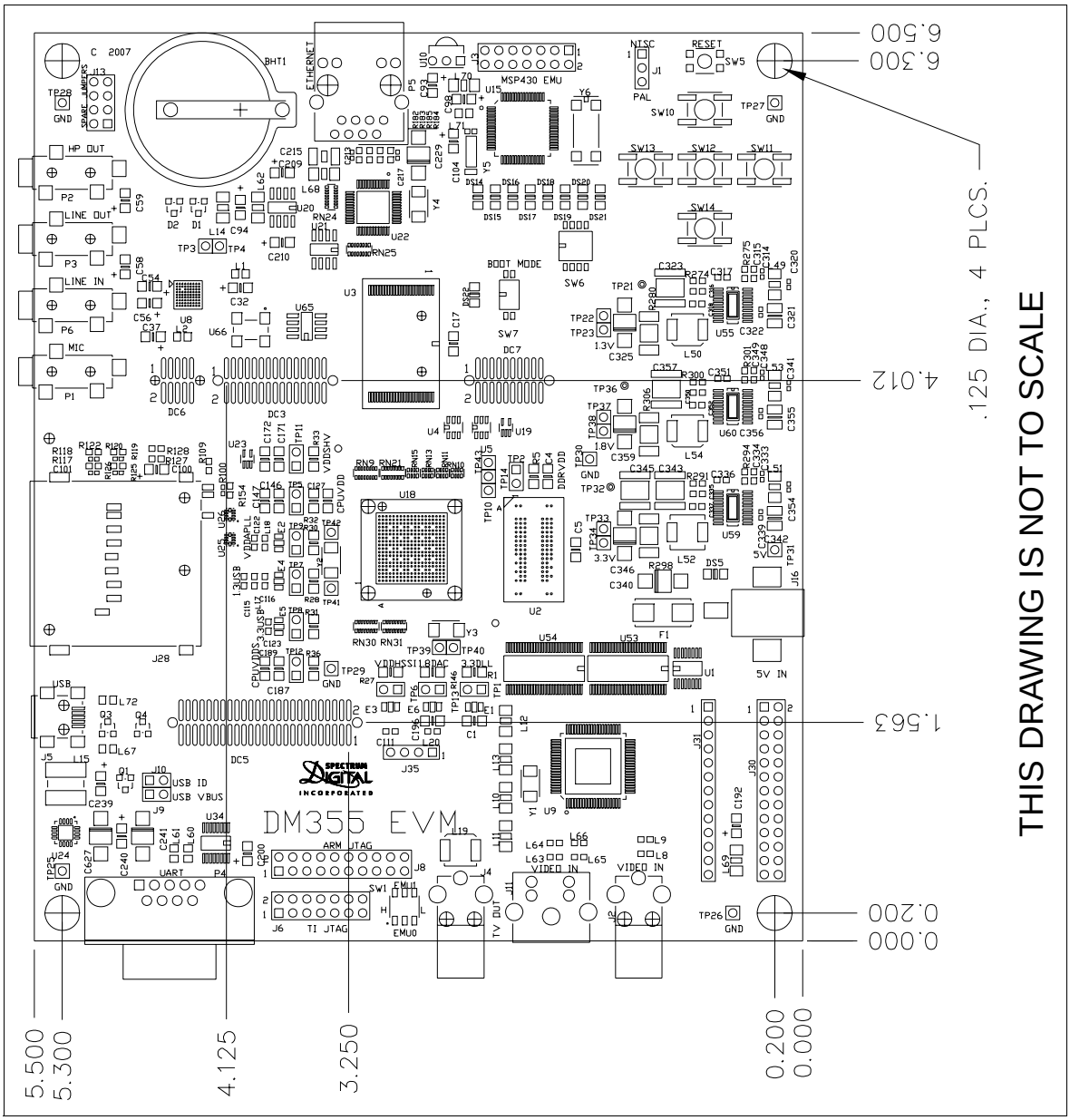

SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: POWER SUPPLY MSP430_3V3, DSP CORE(1V3)
Size:B DWG NO 505902-0001 Revision: A
Date: Friday, March 14, 2008 Sheet 25 of 26
TPS54310PWP
TPS73601QDRG4
BLM41P750SPT
Vout = Vref * (1 + R1503/R1504)
Vref = 1.182 Volts
Vout = 3.6 volts
R1503 = 346K
EMI SUPPRESION , LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.
GND Test Points


SPECTRUM DIGITAL INCORPORATED
Title: DM355 Evaluation Module
Page Contents: POWER SUPPLY 3V3 ,1V8
Size:B
DWG NO 509902-0001
Revision: A
Date: Friday, March 14, 2008
Sheet 26 of 26
TPS54310PWP
101338-0001
BLM41P750SPT
SMCJ6.0A
J16
2.5 MM JACK
RASM712
F_4.0A
GREEN
3V3_PWR_OK
1V8_PWR_OK
3.3 @1.5Amp Max
EMI SUPPRESION, LOCATE NEAR EACH REGULATOR. 6 VIAS FROM PAD TO PLANE OR DIRECT TIE.
22 MSP430_3V3_ENABLE
22 MSP430_1V8_ENABLE

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM355 EVM produced by Spectrum Digital.


THIS DRAWING IS NOT TO SCALE
.125 DIA., 4 PLCS.
6.500
6.300
4.012
1.563
0.200
0.000
5.500
5.300
4.125
3.250
0.200
0.000
DM355 EVM
SPECTRUM DIGITAL INCORPORATED
MSP430 EMU
ETHERNET
BHT1
HP OUT
LINE OUT
LINE IN
MIC
USB
UART
ARM JTAG
TI JTAG
VIDEO IN
TV OUT
BOOT MODE
NTSC
PAL
RESET
5V IN
USB ID
USB VBUS
SPARE JUMPERS

[redacted]

SPECTRUM DIGITAL INCORPORATED

Printed in U.S.A., April 2008
509905-0001 Rev E